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Evaluation of Multilayer Printed Wiring Boards by Metallographic Techniques

An Illustrated Guide to the Preparation and Inspection of Plated-Through Hole Test Coupons Based on the Requirements of MIL-P-55110D

Jane Jellison

NASA

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Evaluation of Multilayer Printed Wiring Boards by Metallographic Techniques

An Illustrated Guide to the Preparation and Inspection of Plated-Through Hole Test Coupons Based on the Requirements of MIL-P-55110D

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INTRODUCTION

This report has three purposes: 1) to promote an awareness of the need for the evaluation of multilayer printed circuit boards (MLBs) prior to acceptance and use, 2) an appreciation of some of the problems encountered in their evaluation, and 3) to furnish guidelines for the preparation and interpretation of metallographic cross-sections of MLB plated-through-hole coupons. It is prompted by several years' experience in reviewing MLB plated-through hole test coupons by microsection examination, with many of these reviews following in the wake of a plated-through hole problem encountered on a fully populated and assembled MLB. It is intended as an aid and guide to all those who are concerned with the reliability of multilayer boards: spacecraft and instrument technical managers, quality assurance inspectors, and to the laboratory support personnel upon whose efforts depends the success of the entire evaluation procedure.

No attempt is made to pinpoint the causes of observed defects nor to suggest remedies: that is beyond the scope of this report. The emphasis is on the metallographic preparation and interpretation of MLB plated-through hole test coupon microsections based on the requirements of MIL-P-55110,"Printed Wiring Boards." Other aspects of MLB quality conformance inspection which either require less subjective interpretation or are not usually performed in the metallographic laboratory, are not treated. The current version of MIL-P-55110 is Revision D, dated 31 December 1984.

PART I
THE NATURE OF THE PROBLEM

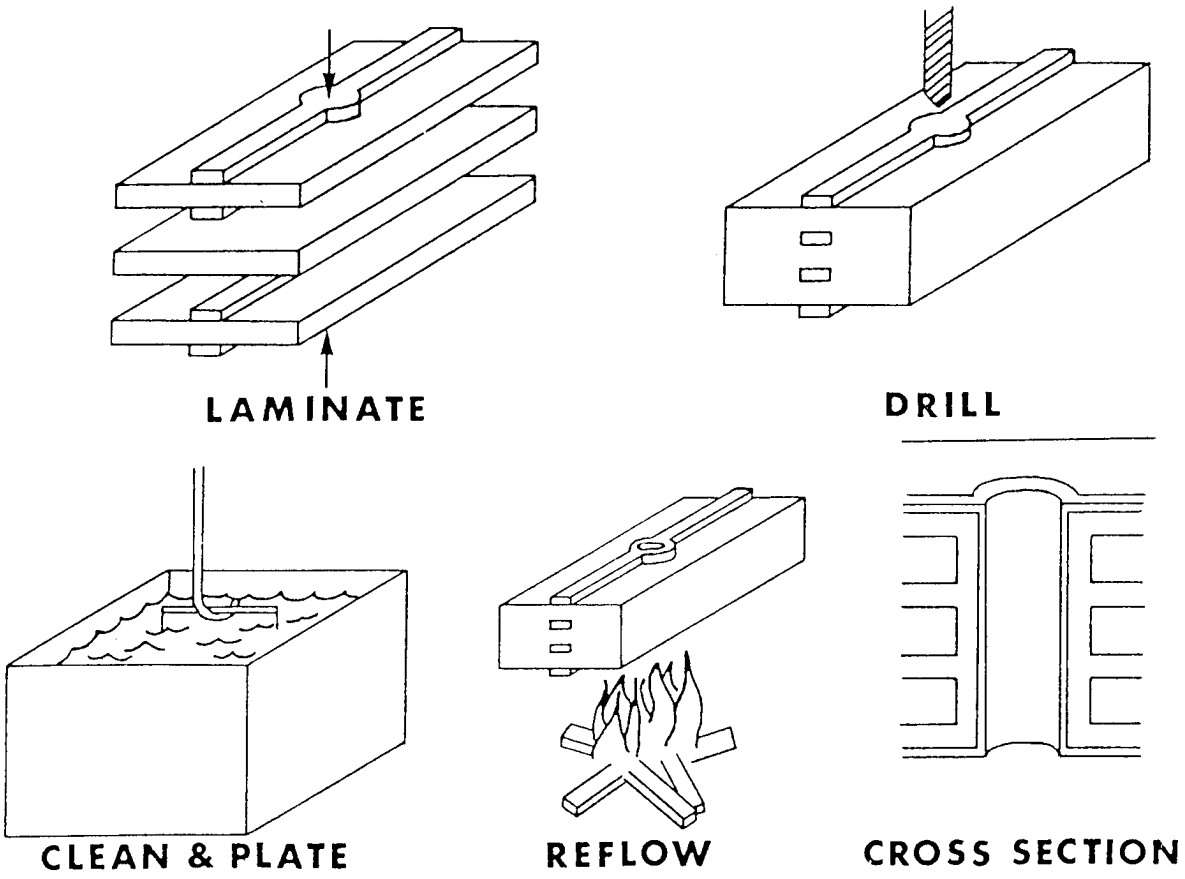
Background

During the past several years, a number of serious problems with MLBs have arisen on various spacecraft and instruments, severely impacting mission schedules and reliability. A few years ago, multilayer board defects forced the last minute removal from flight consideration of a major scientific instrument. Fortunately, the instrument scheduled for the next flight contained good quality MLBs and was available for substitution. In another case, a spacecraft computer exhibited malfunctions on the launch pad which were traced to faulty MLBs. The computer was removed, repaired (by hard-wiring around the defective holes), and reinstalled within three weeks of the launch date. Indeed, multilayer board problems have been encountered on numerous projects over the past several years, and are still occurring. Most of those problems are detected when system performance anomalies arise during or following electrical or environmental (usually thermal cycling) testing. However, at that point it is extremely difficult in terms of both schedule and parts availability to replace the defective boards or indeed to do anything beyond wiring around the faulty area and hoping for the best. To understand why these problems arise so far downstream it is necessary to have a knowledge of the materials of construction and the fabrication and inspection procedures for MLBs.

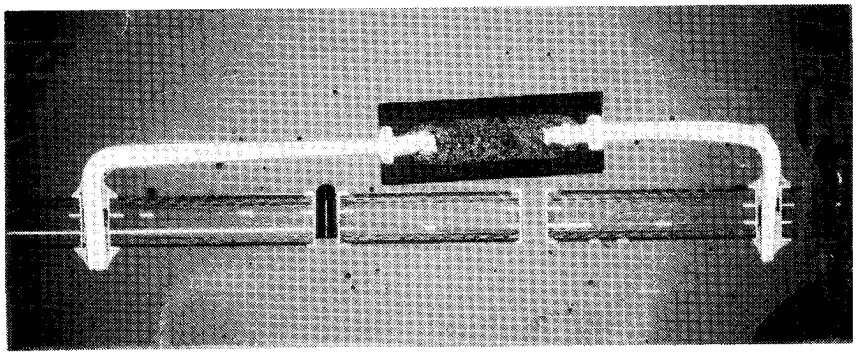
Multilayer Board Construction

A multilayer board by definition contains one or more internal circuit layers. These layers are fabricated separately and then are stacked and laminated under heat and pressure. Usually the stack will consist of alternating fully cured (C-stage) fiberglass-epoxy sheets with copper foil circuitry on both sides and partially cured (B-stage) fiberglass-epoxy spacers (also called pre-preg). During lamination, the B-stage flows and bonds to the double sided elements and cures to form a solid mass of fiberglass-epoxy, referred to as "the laminate" or "the dielectric," with the internal conducting patterns fully encapsulated. To provide electrical continuity among the layers and/or to provide places to mount components, holes are drilled, metallized, and plated with copper. A layer of solder is usually applied for oxidation resistance and for solderability. The final steps are to fuse or reflow the solder plating to relieve stresses and to assure complete coverage, and to cross-section a representative set of holes for quality verification. This process is shown schematically in Fig. 1, and typical cross-sections are presented in Fig. 2. For an excellent overview of the design, production, and quality assurance of MLB fabrication, written for the layman, see "Printed Circuit Technology," by Norman Einarson (1).

A variety of defects can arise during processing: laminate voids, mis-registry of layers, inadequate interlayer spacing, failure of hole (barrel) plating to adhere to the ends of the inner copper foil circuit traces (innerplanes), improper plating thickness and quality. All of these defects are internal, and not readily detected. Many are latent in nature, and do not become apparent until some stress is



SCHEMATIC REPRESENTATION OF MAJOR STEPS IN MULTILAYER BOARD FABRICATION

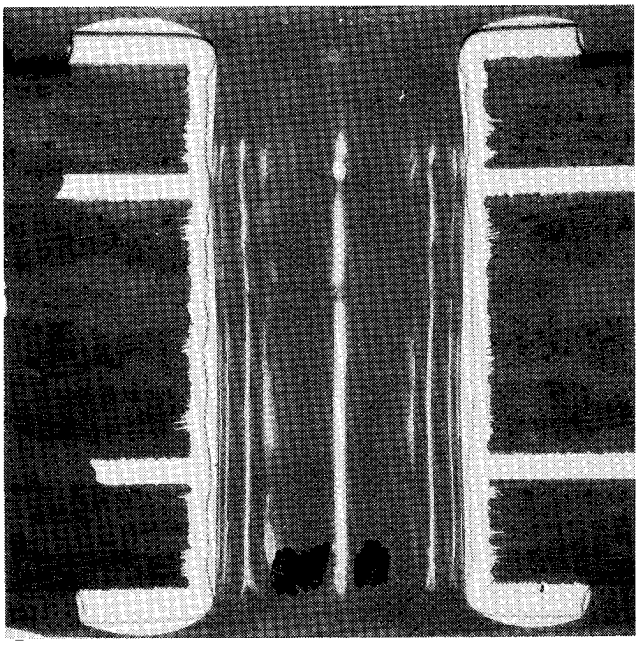


CROSS-SECTION THROUGH A RESISTOR MOUNTED ON A 4-LAYER BOARD.

Figure 1. Multilayer board construction.

CROSS-SECTION OF HOLE AT 50X.

HOLE EDGES SMOOTH, PLATING OF UNIFORM AND ADEQUATE THICKNESS; NO VOIDS IN LAMINATE



DETAILS OF ONE SIDE OF A HOLE AT 175X.

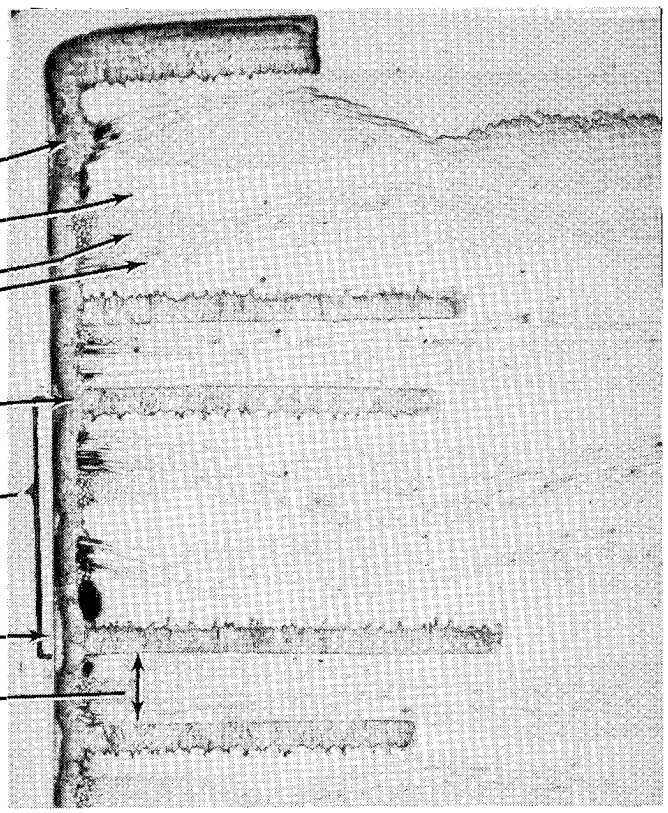


Figure 2. Cross-sections through good quality plated-through holes illustrating typical appearance and nomenclature of elements of construction.

applied to the board. The most common form of stress is associated with soldering or thermal cycling and arises from the widely differing coefficients of thermal expansion of the materials of construction. Changes in electrical parameters go unnoticed until the board has been populated with expensive and frequently irreplaceable (within time and budgetary constraints) components and performance testing has begun. It is this latency, coupled with the difficulty of inspecting MLBs, which gives rise to unexpected problems during testing or to premature service failures.

At first glance, it would seem to be a straightforward case of poor specifications and/or quality assurance procedures which would allow these defects to come to light so late in the long and complex process of producing a viable instrument or spacecraft. But a closer study shows that the inspection procedures best suited to MLB qualification are not easily quantified but rely equally on the skill of the person who prepares the test coupons and the subjective judgment of the inspector.

Problems Encountered in Inspection of MLBs

Unlike most electronic components, which have well defined electrical properties and come in standard part types, MLBs tend to be uniquely designed for a given application, and individually processed. Since the boards are usually made singly or in very small lots, and since the processing parameters are many and difficult to control, virtually every board should be examined for internal quality before components are assembled to it.

Test fixtures which are capable of detecting shorts or opens can be configured for a given board design, but it is usually not practical in terms of cost effectiveness for the very small lot sizes typical of multilayer board procurements for spacecraft and instrument applications. Manual testing is extremely tedious because of the usual complexity of the circuit design, different on each layer, and the difficulty in determining the length of the run, and hence the expected resistance, between any two holes on a given board. In addition, this type of testing does not reveal latent defects, such as weak or partly separated junctions between the hole or barrel plating and the innerplanes which might subsequently worsen under applied thermal stresses. The best method for evaluating the reliability of a MLB is to look inside–to cross section and metallographically examine the internal layers. Unfortunately, this method is destructive in nature and obviously cannot be used on the finished product. What can be done, however, is to dissect a set of holes which is representative of the holes on the board in question, and this method is called out in the customarily used military specification, MIL-P-55110, The current version is MIL-P-55110D, and this is the version which will be referenced in this document.

Each panel (a panel is the unit of fabrication–it may contain only one board or be subsequently cut up into two or more separate boards) is required to contain one or more sets of test holes and circuits which are processed integrally with the boards on the panel and are then removed for destructive testing, such as solderability, rework simulation, and cross-sectioning of the plated-through holes. MIL-P-55110D requires that the microsection inspections be carried out in accordance with ASTM B-487, IPC-TM-650, Method 2.1.1., or by automatic microsectioning techniques. The ASTM method states: "This test method assumes that the individual making the measurement is an experienced metallographer," and goes on to note "the accuracy and reliability of this method are highly dependent on individual technique and skill. Experienced personnel and a microscope of good quality are prerequisites to accurate measurements." There is no mention of what "good quality" means, nor of any procedure to qualify the "experienced personnel." The IPC method details specimen preparation to some degree but also assumes metallographic competence. Although not explicitly referenced in either of these methods, automatic techniques also require skill and experience on the part of the operator to produce a "legible" microsection. Some board manufacturers do not have metallographic laboratories with full technical support but instead rely upon persons with minimal metallographic background to perform this critical inspection step.

In fairness to those preparing and examining MLB coupons, it must be recognized that MIL-P-55110 is not easy to follow with respect to test coupon examination. The current version (Revision D) has been somewhat improved, but it is still a circular document, with second and third generation sub-paragraph references which require persistent detective work to determine just what needs to be done. Later sections of this report will present a suggested guide through the appropriate sections of this specification.

For these reasons, there have been numerous instances of poor implementation of the procedures for plated-through hole inspection which have been uncovered in the course of failure analyses carried out at the GSFC Metallography Laboratory. Some of these are detailed below so as to emphasize the need for close attention to the details of the MLB coupon examination.

Case Histories

1. *Insufficient Sampling:* For multilayer boards, MIL-P-55110 requires that one coupon per panel be cross-sectioned. However, numerous panels with the circuit board cut out but with the entire test coupon intact were submitted for evaluation by several different flight programs after they had become aware of the spacecraft computer problem mentioned above. In many cases, these

boards had been populated or were being worked on at the time the coupons were submitted. Of the coupons submitted, several were clearly unacceptable. It is not known to what specification the boards were built, or what sampling schedule was followed by the vendors, or if indeed any metallographic inspection at all was performed.

Plating baths can become exhausted or contaminated, drills become dull, alignment fixtures slip, or ovens overheat, between the processing of one panel and the next. Therefore, for critical applications (and most MLBs qualify), the coupon(s) from each panel should receive careful examination. This work should be done by the manufacturer at various stages of production so that valuable time is not wasted on a panel which shows serious shortcomings at an early stage. Given the history of problems encountered, however, it seems prudent for the buyer to request documentation of the metallographic inspection, or to have it verified by independent examination. Adherence to the sampling and microsectioning requirements of MIL-P-55110 or another appropriate specification must be emphasized.

2. *Lack of Thermal Stressing Before Sectioning:* At least one severe thermal stress cycle, to simulate soldering operations, is necessary prior to metallographic examination. In one case, failures occurred on completed boards from separation of the through-hole plating from the ends of the inner copper foil conducting layers. Cross sections prepared by the contractor of coupons from the failed board and from many other boards in stock showed clearly that the bonding in these areas was poor, while the vendor maintained that his cross sections looked good. It turned out that the vendor's accept/reject examination was carried out after solder plating the boards, but before the solder was fused or reflowed, and that the coupon had not been subjected to a thermal stress (solder float) test as required by the military specification, so that the appearance of the coupon did not reveal the latent defect brought out subsequently by solder related thermal stressing.

Double-sided boards with plated-through holes should not be neglected in this respect. Although production boards and as-received coupons are easier to inspect from the outside because they have no internal circuit layers, after solder float testing, any cracks which might have formed in the through-hole plating would be covered with solder and hence not detectable by visual examination. MIL-P-55110 does not require 100% microsection inspection for double-sided boards, but for the one-of-a-kind, critical applications encountered in many spacecraft applications, reliability would be enhanced by solder float testing and microsectioning a coupon from each panel.

For example, a double-sided board with plated-through holes was submitted for evaluation of a solder flowthrough problem. In the course of the investigation, corner cracking was observed in some of the holes which had component leads soldered into them. With adequate solder flow, wetting the lands on both sides of the board, this condition, although undesirable, could probably be tolerated. However, should such cracking occur in a hole which the solder did not completely fill, an open circuit could result, either immediately (which should be detected by functional testing of the board), or, more dangerously, at some time in the future if a partial crack were to propagate because of thermal cycling during service. A review of the extant microsections, which were mostly in the as-received condition, revealed no major defects, although some of the copper plating microstructures were not of the most desirable sort. When coupons were solder float tested and microsectioned, many instances of cracking were noted. Since most of the instrument containing these boards was already built, an extensive repair of the defective boards was required, leading to schedule impacts as well as expense.

3. *Poor Quality Metallograhy:* In another instance, the vendor was performing metallographic cross-sectioning at the appropriate manufacturing stages, but the technique was so poorly carried out that serious defects were masked by smeared copper filling in the separations between the innerplanes and the barrel plating. Again, the problems did not surface until populated boards were turned on and tested.

Metallographic techniques are difficult to quantify, and although the cited IPC microsectioning specification has been improved, the rationale for certain procedures is not given. For example, some specimen potting materials are applied at elevated temperature and pressure, and some are applied at ambient temperature and pressure. IPC-TM-650 Method 2.1.1 specifies the latter type of mounting material but does not say why. After it had been discovered that the multilayer boards described in Item 2 had been sectioned with no solder reflow, GSFC directed the vendor to section additional holes taken from the coupons after solder float testing. This test consists of floating the coupon on molten solder in order to simulate actual thermal gradients occurring during installation of components. Again, the vendor reported that the coupons looked good, while those portions of the same coupons prepared by GSFC and the contractor showed large separations at the barrel plating/innerplane junctions: the specimen mounting process chosen by the vendor had subjected the coupons to 150 C and 4000 psi, effectively closing the separations opened up by the thermal stress.

In other instances, properly prepared and polished specimens were not etched to reveal a defective microstructure in the copper plating, which subsequently led to brittle failure in the barrel plating. The inverse problem is also frequently encountered: the specimen is etched *before* microscopic examination, and the normal demarcation line between the barrel plating and the foil of the inner layers which is delineated by the etching process obscures indications of poor bonding at these locations. The polished

specimen should be scrutinized at adequate magnification both before and after etching in order to screen for both types of defects.

4. *Inadequate Test Coupon Design:* The underlying assumption with respect to MLB evaluation by test coupon microsection is that the plated-through holes of the test coupon are representative of those on the board, having been processed integrally with it, and removed only after all manufacturing steps have been completed and the board is ready for delivery. Test coupons from each of a lot of six ten-layer boards showed many plated-through hole defects, and the entire lot was rejected. The board manufacturer had performed microsection analysis on a scrap board from the lot and had found no such defects. The difference in appearance was so great that one of the first questions raised was whether the coupons were indeed those of the suspect lot. A review of processing procedures and microsectioning techniques established that they were being properly carried out. The only processing procedure subject to variation was the time at temperature for the tin-lead fusing step. At the operator's discretion, this time may be extended if it appears that the tin-lead has not been completely fused. The board in question had ten layers, four of which were signal layers, and six of which were ground planes, including both surface layers. This is an unusually high number of ground planes, and the presence of so much copper in the board would increase its heat-sinking capacity above that normally encountered. The test coupon, however, while containing the specified layout of plated-through holes, had not been configured to contain any ground planes. A visual examination of the boards and their coupons showed that the coupon laminate was somewhat browner in color than that of the boards, although the board color was difficult to evaluate because of the almost complete coverage by the surface ground planes. This color change suggested that the coupon laminate had been overheated, which correlated with the fact that the types of defects noted in the coupons were those usually associated with thermal stress. Further investigation established that the fusing time had indeed been extended for these boards, with the result that, because of the absence of ground planes in the coupon, it was overheated while the board itself, with its greater heat-sinking capacity, was being correctly fused.

Summary of Problem

Multilayer printed circuit boards are produced singly or in very small lots by complex state-of-the-art manufacturing processes which are subject to daily if not hourly variations and which are difficult to control. Typical defects are internal, quite likely latent, and not amenable to detection by nondestructive means. Procedures exist and are usually specified for examining sample plated-through holes from each panel to detect defects. The usefulness of these procedures is highly dependent upon the skill of the person performing them, and the results are open to subjective interpretation. These acceptance procedures are performed by the vendor, and may not be adequately carried out.

The first portion of this report has been aimed at increasing the awareness of the need for close review of board coupons prior to acceptance and use. The remaining sections will illustrate the major types of defects encountered, using as a guide the sections of MIL-P-55110 which pertain to cross-sectioning of plated-through holes, thus providing a working acquaintance with the appearance of "good" and "bad" holes; and will detail a recommended specimen preparation procedure designed to minimize artifacts so as to provide a valid surface for microscopic examination. It should be noted that there are many procedures, both manual and automatic, which will yield well-prepared specimens, and no single one is so superior that it should be imposed as a requirement. In addition, certain inspection procedures and requirements which exceed those spelled out in the military specification will be suggested.

The applicable paragraphs of MIL-P-55110 are given in their entirety in Appendix A, and the preparation procedure is outlined in Appendix B.

PART II. EVALUATION OF MICROSECTIONS BASED ON MIL-P-55110D

The full quality conformance criteria of the military specification are listed in Table VII, p. A-3. They are divided into five major categories: visual, dimensional, physical requirements, construction integrity (microsection), and electrical and environmental requirements. Most of these require no metallographic expertise, and very likely will not be evaluated by the person who cross-sections the plated-through holes.

Visual inspection is for the most part performed on the production boards (not test coupons) using a binocular microscope at low magnification. Most of the dimensional inspections are also visual in nature, and are performed on the production board as well. The exceptions are layer-to-layer registration for most type 3 (multilayer) boards, solder mask thickness (when present), and plating and coating thickness. These latter two inspections may be carried out either on the board or on a test coupon at the manufacturer's option. The plating and coatings referred to are gold, nickel, tin-lead and solder, not the copper plating in the hole. Tin-lead plating and solder coating must be measured prior to fusing or reflow. Since most boards and their associated coupons have been fused or reflowed before they reach the metallogaphy laboratory, these measurements are seldom performed as part of the microsection portion of acceptance testing. Physical and electrical requirements are also usually evaluated outside of the metallography lab.

What *is* done in the metallography lab is the evaluation of construction integrity by microsection examination,

both as received and after thermal stress, and it is to this area that the emphasis of this document is directed.

The paragraphs of MIL-P-55110D relating to microsectioning of test coupons have been picked out and arranged into a format more easily followed by the metallographer who is preparing and examining the plated-through hole microsections. Most of the discussion will concern type 3 (multilayer) PTHs, but some paragraphs pertaining to type 1 (single sided) and type 2 (double sided) boards have also been included. This compilation is presented here as Appendix A. The original paragraph, figure, and table numbering has been retained to facilitate reference to the complete military specification, except that figure numbers have been preceded with an "A."

The definitions of terms listed in MIL-P-55110D are presented first (paragraph 6.7), followed by the full listing of quality conformance inspection criteria (paragraph 4.7) as detailed in Table VII, "Group A Inspection," and Table IX, "Group B Inspection." In these tables, paragraphs which concern microsectioning and which are included in Appendix A are marked by asterisks. Additional paragraphs which are referenced in the primary paragraphs are also included in Appendix A. The relevant paragraphs are presented in Appendix A in the order in which they are referred to in the specification, with the requirements (paragraph numbers beginning with a "3") starting at the left margin, and the methods (paragraph numbers beginning with a "4") offset beneath them. All paragraph numbers referred to in the balance of this report are those of MIL-P-55110D unless otherwise identified.

For multilayer boards, Group A testing requires that 100% inspection (i.e., one coupon per panel) be carried out on one portion of test coupon B in the as-received condition (paragraph 3.8), and on another portion after thermal stress (paragraph 3.9). Group B testing is performed on sample units which have passed Group A testing. The paragraphs of metallographic interest in group B cover rework simulation (soldering and unsoldering of wires into hole) and subsequent microsection examination. Most routine MLB examinations will be concerned with Group A inspection, and those tests will be given major emphasis here.

Test: Layer-to-layer registration (3.6.6, 4.8.5.3, Fig. A-1)
Requirement: 0.014" misregistration maximum

There are three possible means of making this measurement: by microsection examination (coupon F for multilayer boards), by test of special registration coupons, or by visual assessment (production boards for double sided and certain multilayer boards).

Method 1: Microsection examination (3.6.6, 4.8.5.3.1). Coupons from two diagonally opposing corners of the panel are prepared in vertical cross-section, one taken in the length direction of the panel, and the other in the width direction. [In most cases, only one coupon will be furnished to the metallographer. In this case, specimens oriented parallel and perpendicular to the coupon length should be prepared.] The measurement is done at 100X ±5%. External and internal lands are included in the evaluation. The centerlines of the two lands on each section which are most laterally shifted with respect to one another are determined, and the distance between these centerlines is the amount of misregistration. This procedure is illustrated in Figure A-1.

Method 2: Special Registration Test Coupons (3.6.6.1, 4.8.3.5.2). Special registration test coupons may have been designed into the panel. Criteria for these will be specified on the master drawing. Each case must be considered separately and this method will not be discussed here.

Method 3: Visual assessment (3.6.6.2, 4.8.3.5.3). The provision for visual assessment of registration is new with this revision of MIL-P-55110, and applies to double sided and some multilayer boards. For double sided boards, registration is deemed satisfactory if both sides of the board meet the criteria for minimum annular ring (3.6.7, 4.8.3.6) [see below] and hole pattern accuracy (3.6.2, 4.8.3.1; required to be as specified on the master drawing). This latter measurement is to be done on the production board by visual examination at 4X minimum.

Multilayer boards with six or fewer layers which meet the external annular ring criteria may be inspected using a combination of top and bottom (transmitted) light, provided that the following conditions are met: a) each internal layer must be observable from one or the other side of the board, b) it must be visually comparable, land for land, to the surface pattern at a minimum of two through-hole locations, and c) these two locations must span at least 80% of the diagonal length of the land pattern. If these conditions cannot be met, the registration must be evaluated by microsection examination (Method 1 above).

Test: Annular Ring (external) (3.6.7, 4.8.3.6)
Requirement: a) Single sided – 0.015" minimum
b) Double-sided and multilayer – 0.002" minimum, except 0.005" adjacent to conductor run.
Method: Measured on production board at 4 – 10X; graphically defined in Figure A-2. The measurement is taken from the inside surface (within the hole) to the outer edge of the annular ring on the outside. A 20% reduction of the minimum requirement is permitted in isolated areas. No mention is made of measurement on a PTH coupon, although the external annular ring is included in the layer-to-layer registration determination, and its measurement is shown in Figure A-1.

Test: Solder Mask Thickness (3.6.8, 4.8.3.7)
Requirement: 0.001" minimum, unless otherwise specified on the master drawing.

Method 1: Measure with any indicator or micrometer accurate to 0.0003".

Method 2. Measure on microsection (coupon E) at 100X ± 10%.

Test: Plating and coating thickness (3.6.9, 4.8.3.8).

Requirement: See Table I, p. A-7.

This evaluation also falls outside of the section dealing with microsectioning of plated-through holes, but may be performed on a microsection. Tin-lead plating and solder coating are only to be measured prior to fusing or reflowing. Most coupons encountered in Group A inspection represent finished boards, and will have been fused or reflowed, so that this measurement is not commonly made during incoming inspection. After fusing or reflow, solderability requirements (IPC-TM-840 Class 3) must be met, but this test requires specialized equipment and is not usually done in the metallographic laboratory. An as-plated tin-lead coating, when viewed in cross-section, will be of uniform thickness, Figure 3a, while a fused coating has a characteristic rounded contour, as shown in Figure 3b. After fusing or reflow, the solder coverage should be complete, not counting the vertical conductor edges.

Method: Solder coating or tin-lead plating is to be measured at least 4 times, once in each quadrant of each panel, or in each quadrant of a microsection.

The other platings covered in this paragraph are gold and nickel. These platings are encountered on plug-in boards where nickel and gold layers are applied to copper plated surface contact fingers for wear resistance/conductivity at the terminal areas, and sometimes on special purpose boards which have nickel/gold overplates over the usual copper traces. An accurate metallographic measurement of these platings (0.000050" minimum for gold and 0.0002" minimum for nickel) is only possible if the coupon has been overplated (typically with 0.001" of electroless or electrolytic nickel) prior to examination.

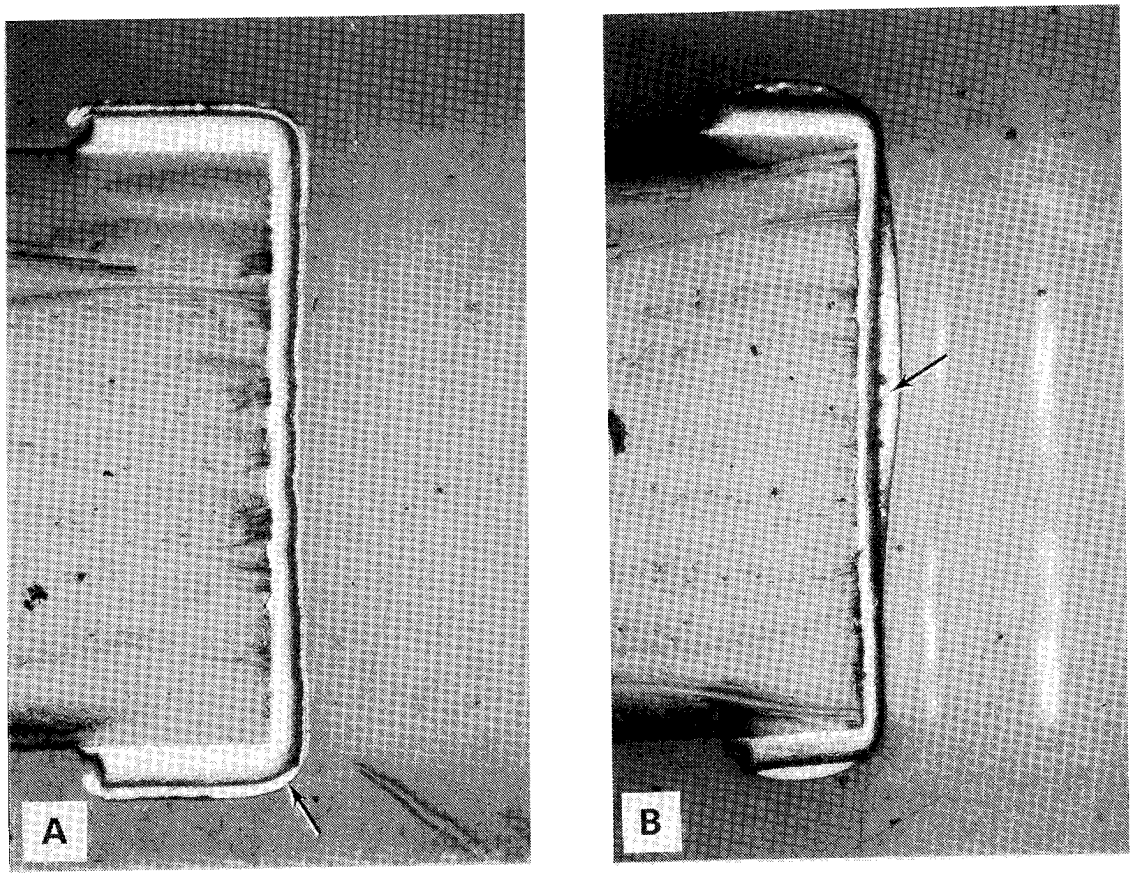


Figure 3. Tin-lead coating:

A. As plated. Thickness is uniform.

B. As fused. Thinner on corners, characteristic rounded contour on vertical hole wall.

Test: Construction Integrity by Microsection ... Prior to Stress (3.8, 4.8.5).

Requirement: Aspects of PTH quality detailed in 3.8.1 through 3.8.11, which will be treated in succeeding sections.

Method: A minimum of three plated-through holes from Coupon B are examined in vertical microsection at the center of the hole ± 10%. The standard magnification is 100X, with 200X used as referee magnification. The various conditions examined are illustrated in Figures A-3 through A-9. Each side of the hole is viewed independently, and measurements are reported as the average of three determinations on each side of the hole. Specimen preparation (4.8.1.2, via 4.8.5.1) is to be accomplished using methods in accordance with either IPC-TM-650, Method 2.1.1, ASTM B-487, or by automatic sectioning techniques. The IPC specification gives a procedure for sectioning, mounting and polishing circuit board coupons; the ASTM specification covers general metallographic specimen preparation and measurement of coating thicknesses, with no reference to printed circuit boards. Adequate specimen preparation can be accomplished by using the IPC specification, but those without a good deal of metallographic laboratory experience may have difficulty in so doing, as well as in interpreting the subsequent observations. A more detailed procedure (Appendix B) has been prepared, and additional tips on printed circuit board specimen preparation are offered (Part III) to augment the cited specifications. The use of these procedures, together with a study of the illustrations provided in Part II, should provide even a newcomer to the field with sufficient guidelines on specimen preparation techniques to enable a valid evaluation to be made.

Plated-Through hole: (3.8.1, Figure A-3). Cracks in the conductive foils, platings or coatings are not permitted, nor are separations at conductive interfaces (such as between adjacent plating layers, or at the junction of the innerplanes and the barrel plating). A crack is a break within a solid mass of material; a separation is a failure to bond, or an opening of a bond.

Figure 4a shows a crack in the barrel plating at the high stress area at the surface of the board. Plating cracks commonly result from brittle hole plating, and frequently propagate around the entire circumference of the hole. Cracks tend to form and propagate most readily at grain boundaries, and plating with a large-grained, columnar microstructure such as that illustrated in Figure 4a is much more prone to cracking than is that which is fine-grained and equi-axed. Moreover, the grain boundaries of columnar type plating are aligned perpendicular to the direction of maximum stress, which is that imposed by the increase in the board thickness caused by the large coefficient of thermal expansion of the epoxy in the laminate. In the plane of the board, the epoxy is restrained by the sheets of fiberglass cloth; in the thickness direction no such restraint exists. The crack in Figure 4a has been bridged by solder during the reflow operation, and electrical continuity testing would not reveal this defect. However, such a hole will have increased electrical resistance, which could be detrimental in high current or low resistance applications. A plated-through hole showing any crack should be rejected. Examination for cracks should be done both before and after etching. Figure 4b shows a corner crack in a double sided board which extends most of the way through the barrel plating. This crack is very tight and was not visible before the specimen was etched. The board which this coupon represents should also be rejected even though the crack does not completely penetrate the plating. Subsequent thermal stress either from rework or from thermal cycling during service could well cause propagation to failure.

Separations may occur between successive layers of barrel plating, Figure 5a, or at the ends of the copper foil layers where the barrel plating bonds to them, Figure 5b. Separations at this latter location are frequently associated with resin smear. Resin smear is exactly what it sounds like: the heat and pressure associated with the drilling operation cause epoxy from the laminate to be dragged over and stuck to the exposed edges of the copper foil of the innerplanes. Unless thoroughly removed in pre-plating cleaning or by etchback (3.8.5, see below), this will prevent good adhesion of the barrel plating to the ends of the innerplanes.

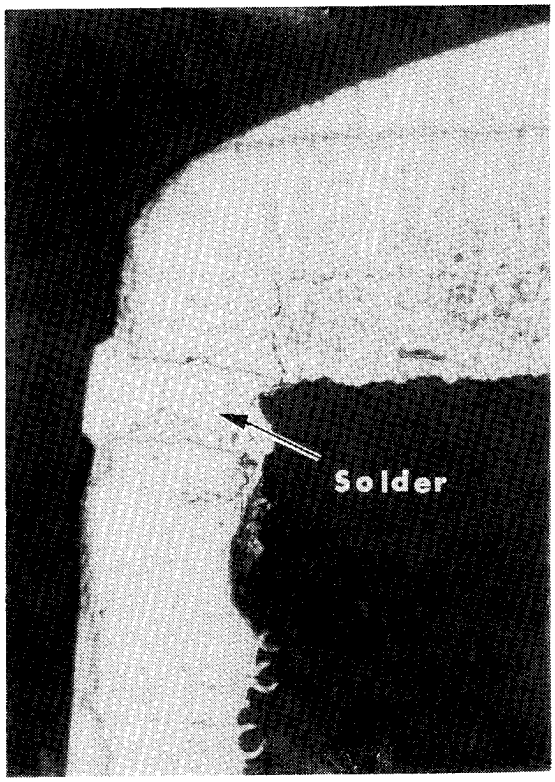
In addition to viewing with increased magnification, the specification calls for a second microsection to be prepared if resin smear is detected or suspected, this time in the horizontal plane (plane of the board), which will reveal the conditions around the circumference of the hole at the foil/plating interface. Figure 6 illustrates two such views.

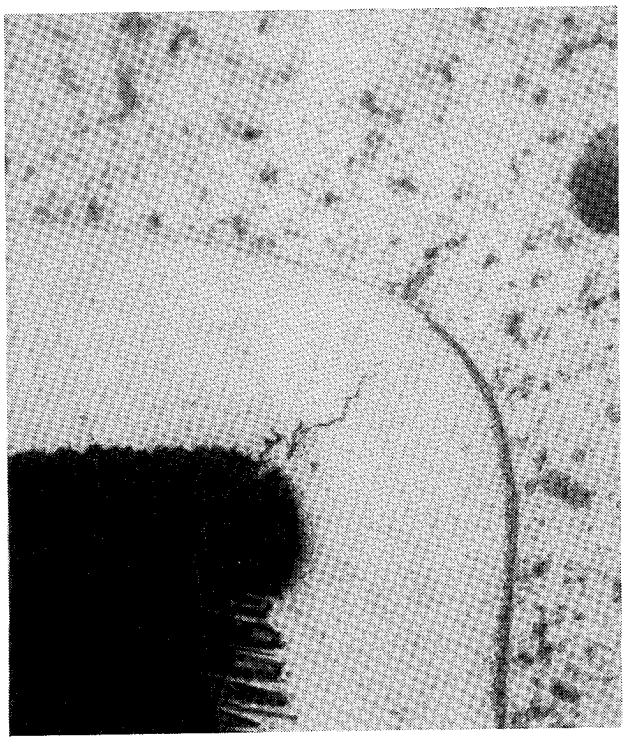
Resin smear is often associated with nailheading. Nailheading (see Figure A-3) is distortion of the ends of the inner foil traces caused by faulty hole drilling techniques such as using dull drill bits, excessive pressure, or improper speed. Poor drilling practice tends to smear excessive amounts of epoxy over the ends of the innerplanes so that the standard hole cleaning or etchback treatments may not remove it all. Nailheading of itself is not harmful and is acceptable provided it does not exceed 1.5 times the foil thickness. Figure 7 gives examples of multilayer plated-through holes with varying degrees of resin smear and separations, all with nailheading of the ends of the innerplanes. The nailheading in Figures 7a and 7c is in excess of that allowed in the specification.

Separations at barrel/innerplane junctions are also often observed which are not associated with any signs of poor drilling practice such as ragged holes, nailheading, or obvious resin smear, see Figure 8. These separations appear to result from a weak bond opening up rather than from no bonding having taken place. This condition was noted in the service failure illustrated in Figure 8b. This hole showed increased resistance after thermal cycling.

A. CRACK IN BARREL PLATING ASSOCIATED WITH COLUMNAR MICROSTRUCTURE. CRACK IS FILLED WITH SOLDER WHICH FLOWED IN DURING REFLOW. MAGNIFICATION 500X.

REJECT.





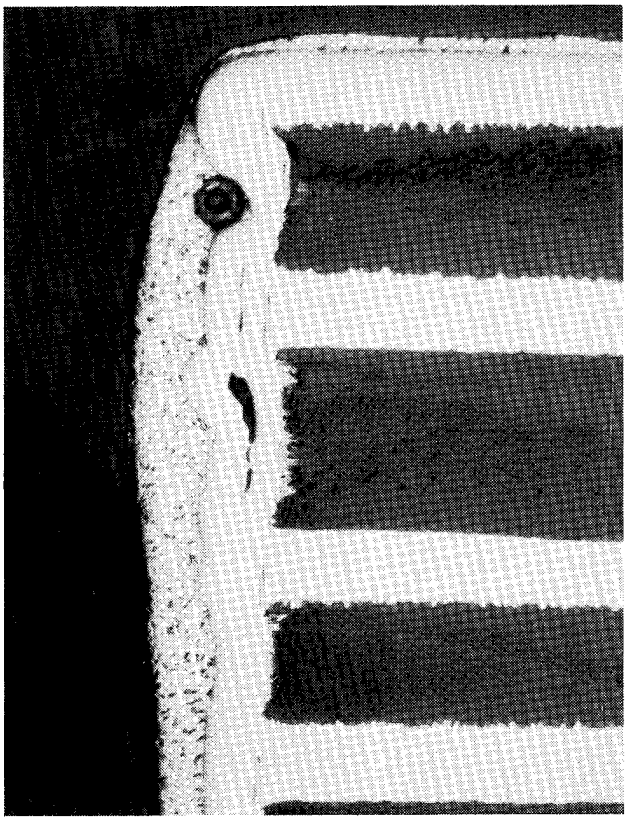
B. TIGHT CORNER CRACK WAS NOT VISIBLE BEFORE SPECIMEN WAS ETCHED. CRACK FORMED DURING SOLDER FLOAT TESTING. MAGNIFICATION 400X.

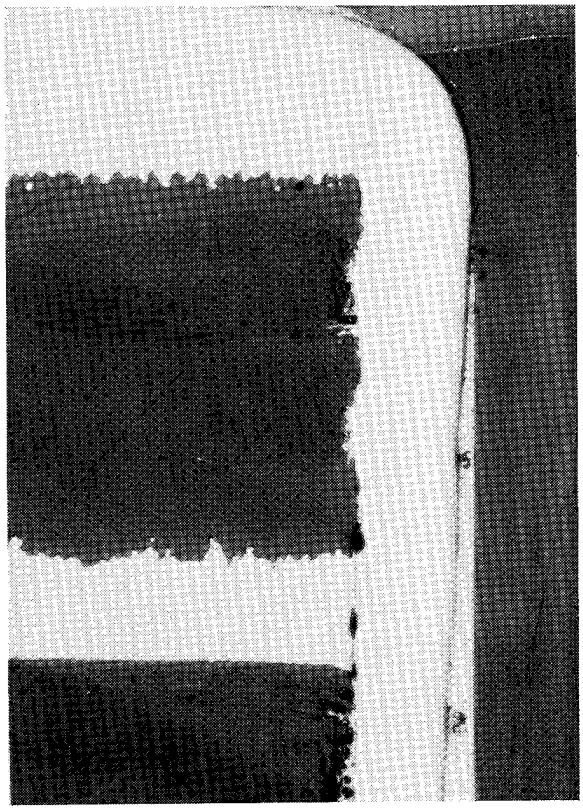
REJECT.

Figure 4. Cracks in barrel plating.

A. SEPARATIONS BETWEEN ADJACENT PLATING LAYERS. UNETCHED. MAGNIFICATION 175X.

REJECT.





B. SEPARATIONS BETWEEN HOLE PLATING AND INTERNAL COPPER CONDUCTORS (INNERPLANES). UNETCHED.

MAGNIFICATION 200X.

REJECT.

Figure 5. No separations are allowed at conductor interfaces.

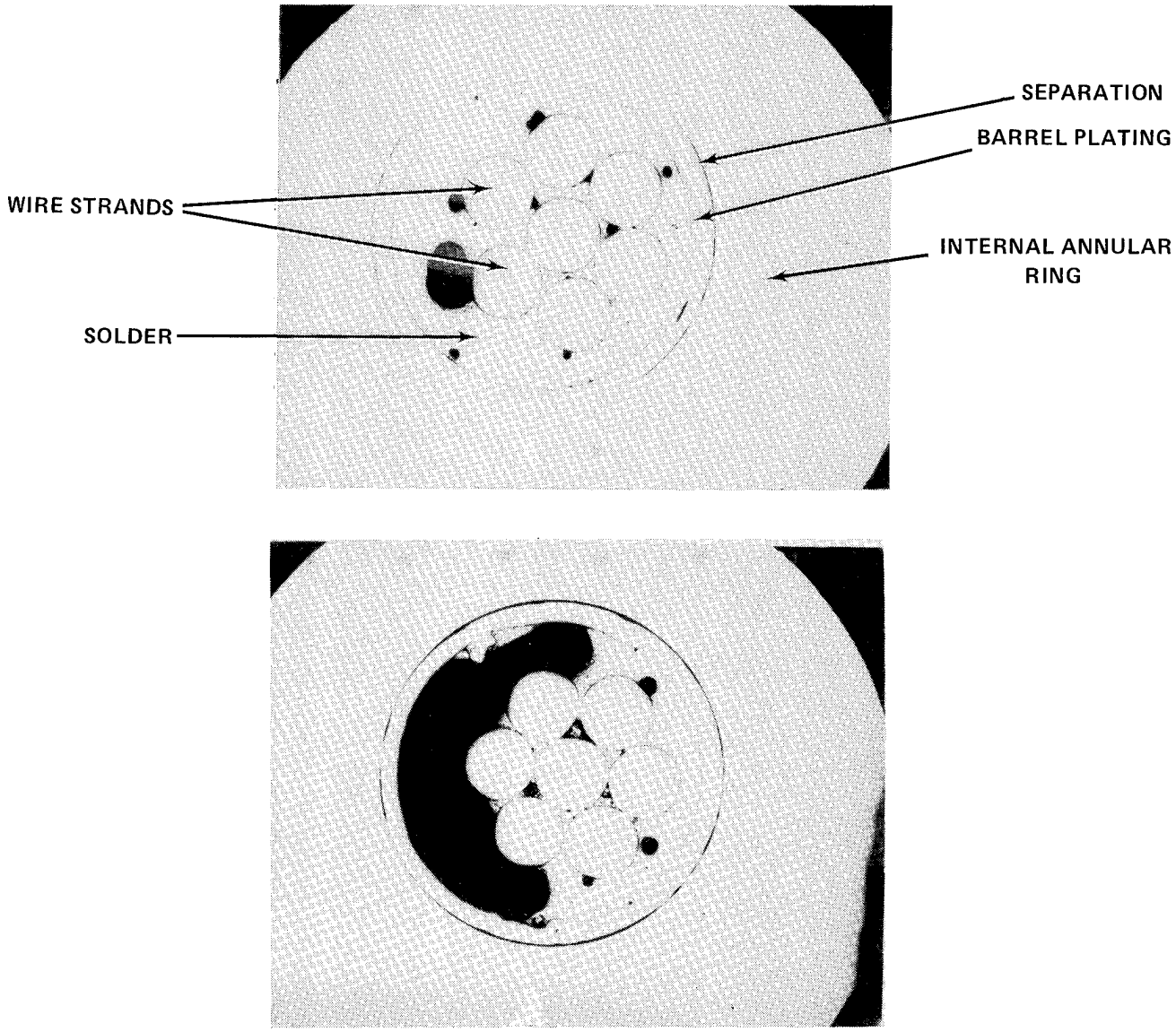


Figure 6. Transverse sections through plated-through holes with stranded wire soldered into them. Separation in upper photograph extends approximately 240 degrees around the hole; that in the lower photo is continuous all around the hole. Both are rejectable. Unetched, 75X.

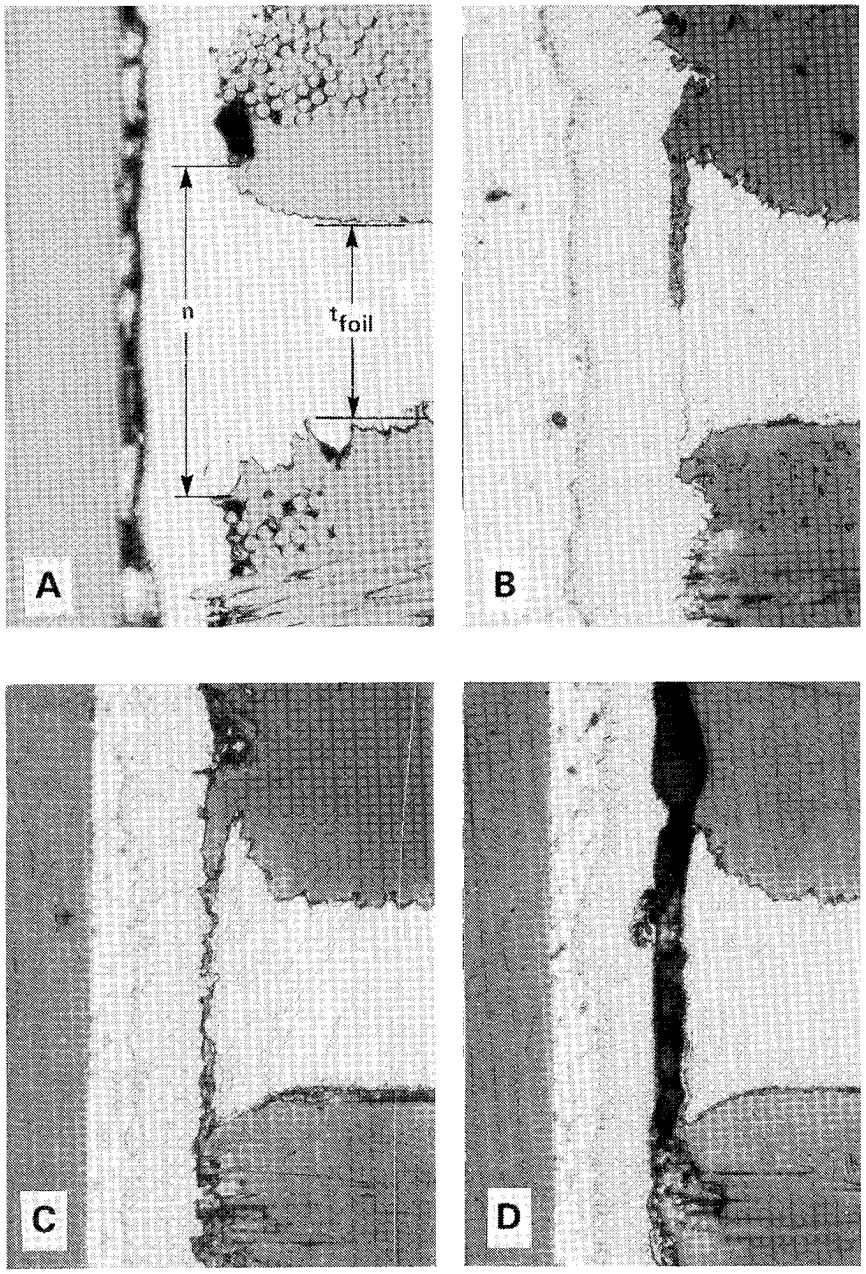
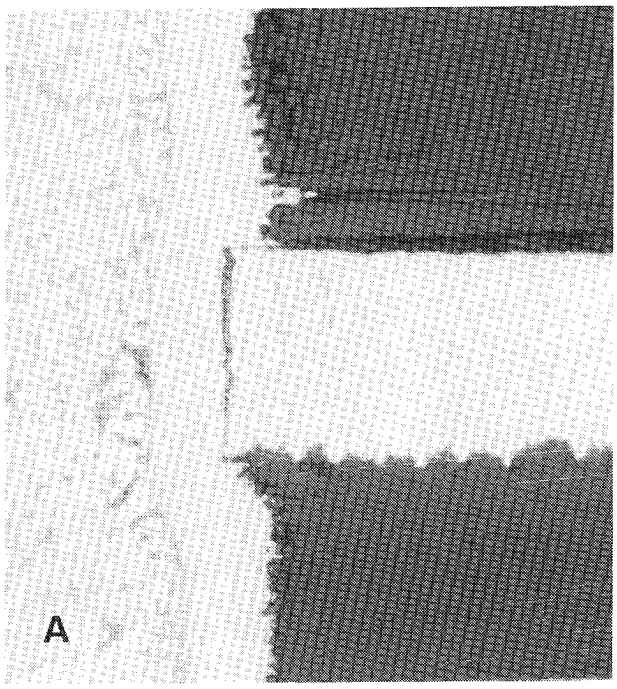


Figure 7. Nailheading is defined as the ratio of the measure of the distorted end of the innerplane to its thickness. Etched, 400X. $N = n/t_{foil}$

A. Nailheading (N) with no resin smear or separation. N = 1.7, in excess of the 1.5 maximum allowed.
B. Nailheading with resin smear. N = 1.6. May be rejected for both conditions.
C. Excessive nailheading (1.7) with separation. Reject for both conditions.
D. Nailheading (1.5) at outer limit of acceptability, but reject for separation.

A. SMOOTH HOLE WALL, NO NAILHEADING, SEPARATION AT BARREL/INNERPLANE JUNCTION. PATTERN INDICATES THAT AT ONE TIME THE PLATING WAS JOINED TO THE FOIL END. UNETCHED. 400X.



B. SERVICE FAILURE. THERMALLY CYCLED HOLE WITH RESISTOR LEAD SOLDERED INTO IT, WITH SEPARATIONS AT BARREL/INNERPLANE JUNCTIONS. HIGH RESISTANCE WAS NOTED AT THIS HOLE.

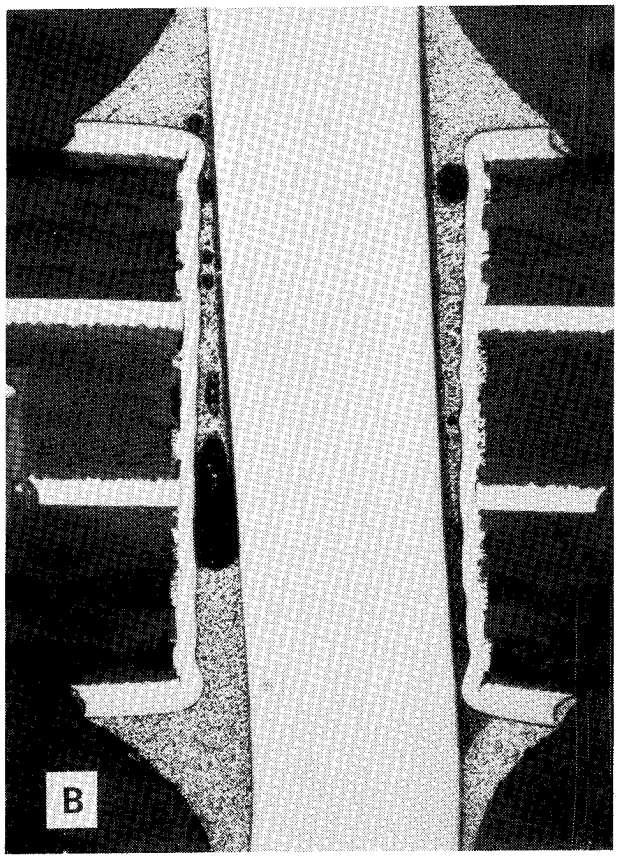


Figure 8. Separations not associated with resin smear or nailheading.

It is sometimes difficult to distinguish between a separation with a thin layer of epoxy between the innerplane and the hole plating (resin smear), and a separation with empty space between them. The distinction is only important when diagnosing the cause of the problem as opposed to merely evaluating the coupon. In addition, although the specification does not specifically address it, a demarcation line visible in the unetched condition at the innerplane/barrel interface is a sign of a weak bond, and coupons exhibiting this feature should be rejected. Examination for separations and resin smear should be carried out before any chemical etching of the specimen is done. Etching may obscure a fine line defect by superimposing on it the normal boundary line between the grain structure of the foil and that of the hole plating which is revealed by the etching process. The referee magnification of 200X is frequently required to clarify conditions at the innerplane/barrel interfaces.

Nodules, plating folds, and glass fiber protrusion are signs of sloppy drilling or hole cleaning prior to plating, and can lead to plating cracks under thermally induced stressing. Nodules may result from plating over an irregular hole surface or may be a sign of a plating bath going out of control. Plating bath composition and operating parameters such as temperature, current density, time in bath, and the physical arrangement of the workpieces in the plating tank all contribute to the quality of the final plating, and should all be closely monitored on a regular schedule. The nodules in Figure 9a are associated with brittle, columnar microstructure which has cracked under thermal stress. Those in Figure 9b and 9c are confined to one surface of the board and probably reflect improper positioning of the electrodes in the plating tank. The nodules in Figure 10 arose when the plating attempted to coat an irregular hole surface which had numerous epoxy lumps which were not removed during the hole cleaning process. Note that the hole illustrated in Figure 9b should also be checked for layer-to-layer registration. It is not infrequent that more than one defect is found on a poorly fabricated board.

Figure 11 illustrates plating folds. The initial electroless copper plating layer followed and adhered to the irregular surface of the hole wall, and the subsequent buildup of electrolytic copper resulted in a folded structure. These sharp folds have high stress concentration factors, and cracks may initiate at these locations. Coupons exhibiting this condition should be carefully checked for cracked plating after solder float testing. Glass fiber protrusion into brittle and/or thin plating may also lead to cracked barrel plating, Figure 12. Plating folds, nodules, and glass fiber protrusion which project into the hole, Figure 13, are acceptable provided the hole diameter is not reduced below what is specified on the master drawing. Since this drawing is not generally available to the metallographer, the presence of nodules, folds, and protrusion should be noted, and the minimum remaining hole diameter should be measured and stated in the evaluation report.

Test: Thermal planes (3.8.1.1, 4.8.5.1)
Requirement: 0.004" minimum
Method: The lateral dielectric spacing between heat sinking planes and adjacent conducting surfaces (nonfunctional lands) or plated-through holes is measured at 100X on the microsection at the closest point between these surfaces, Figure 14.

Test: Plated copper thickness (3.8.2, 4.8.5.2, Figure A-4)
Requirement: Electroless: sufficient for subsequent electrodeposition
Electrolytic: 0.001" minimum
Method: The copper plating thickness in the hole is determined by averaging three measurements on each side of the hole, taken at 100X. The copper plating thickness in the hole should measure at least 0.001". Isolated thick or thin spots should not be used for measurements. Isolated flaws are permitted down to 0.0008". Any isolated areas measuring less than 0.0008" are treated as voids (Figure 15).

Inadequate plating thickness may or may not be associated with other defects. The hole plating in Figure 16a is uniform and has good microstructure, but is too thin; it has cracked because it lacked the strength to withstand the thermally induced strain from the solder float test. Quite frequently, however, thin plating is observed on rough, irregular hole surfaces, and arises from hole drilling problems rather than plating bath faults, Figure 16b.

Acceptable holes with good barrel plating are illustrated in Figure 17. The number of layers of barrel plating is not significant. The initial metallizing layer is only angstroms thick and is not visible in cross section. The electroless copper applied next is also normally too thin to be seen. An electrolytic copper strike layer may be visible, together with one or more electrolytic layers applied to build up the full thickness of plating. The nailheading in Figure 17b is within acceptable limits.

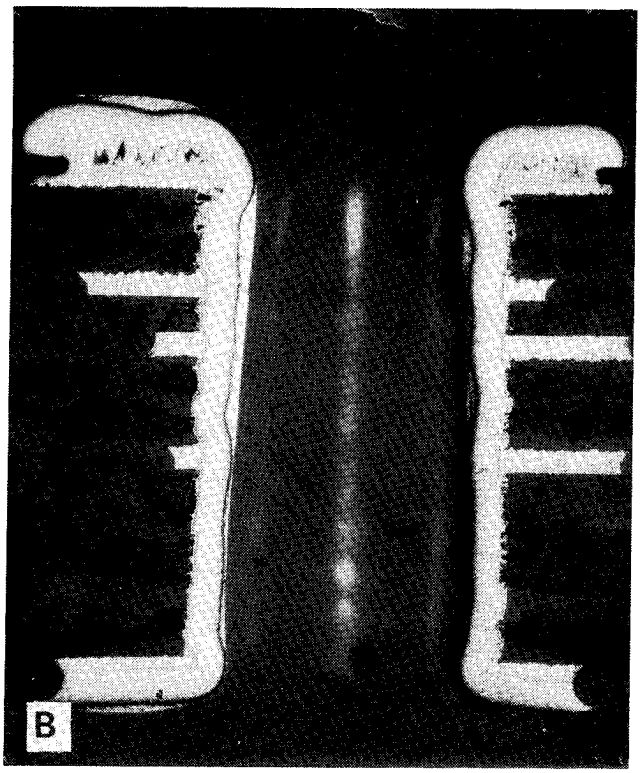
Test: Plating voids (3.8.3, 4.8.5.3)
Requirement: No more than 3 in one hole; none at interconnections; none in same plane on opposite sides of a hole (Figure A-5 shows microsection requirements). Combined length of voids not to exceed 5% of total wall length; combined area not to exceed 10% of total barrel surface area; no circumferential voids (visual inspection requirements).
Method: The microsection is inspected at 100X. If voids are present in the microsection, the lot is to be 100% visually inspected.

Plating voids are discontinuities in the barrel plating. None are allowed in the same plane (opposite sides of a hole at the same layer) or where the hole plating meets an internal conductor; there must be no more than three in one hole. The combined length of voids must not exceed

A. NODULES ASSOCIATED WITH BRITTLE PLATING PROBABLY RESULT FROM PLATING BATH COMPOSITION PROBLEMS. THE NODULES WOULD BE ACCEPTABLE; THE CRACKS ARE NOT. ETCHED, 500X.

B. NODULES IN ONE PLATING LAYER ON ONE SIDE OF THE BOARD MAY RESULT FROM IMPROPER POSITIONING OF ELECTRODES DURING PLATING. ETCHED, 50 X.

C. HIGHER MAGNIFICATION VIEW OF HOLE ILLUSTRATED IN B. ETCHED, 175 X.



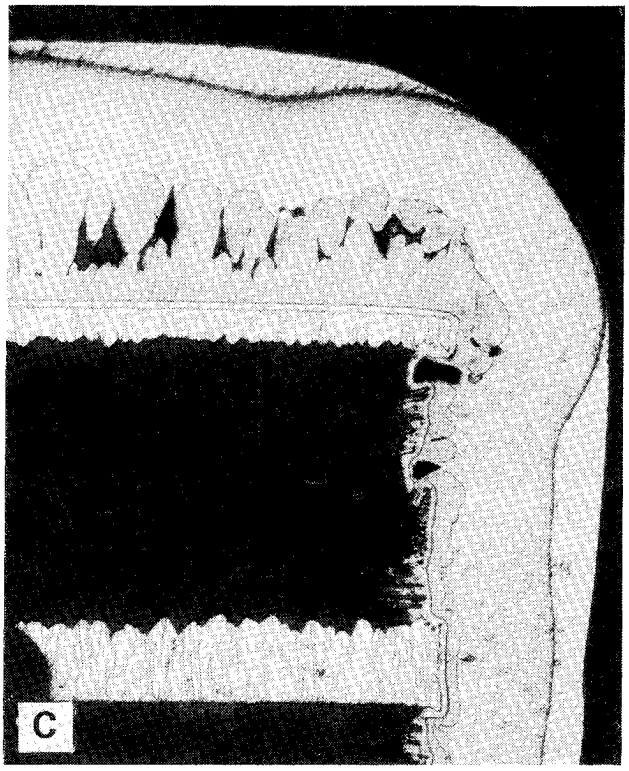


Figure 9. Examples of plating nodules in barrel plating.

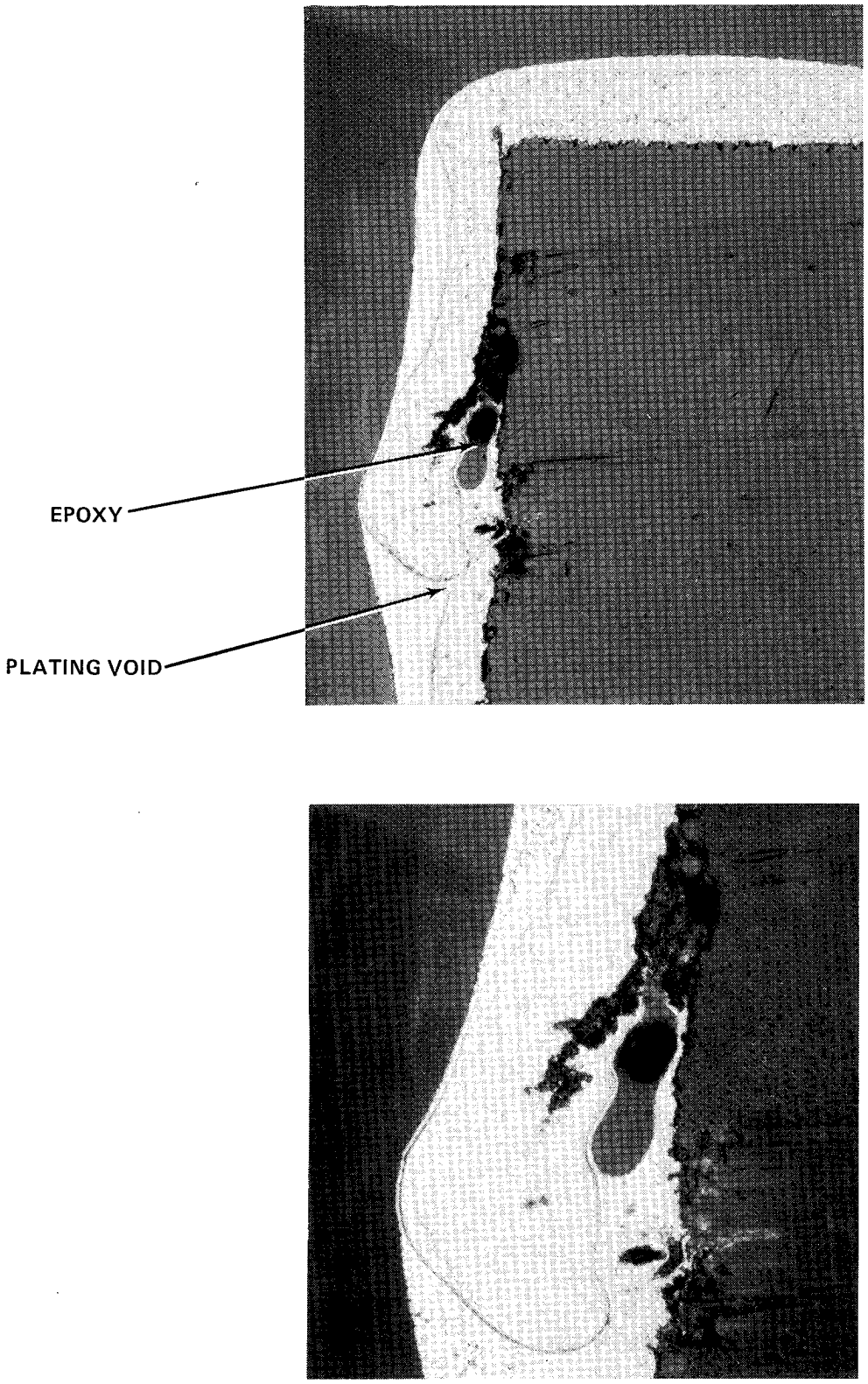


Figure 10. Nodules which formed on rough hole wall have led to a plating void. Etched. Upper photo at 200X; lower at 400X.

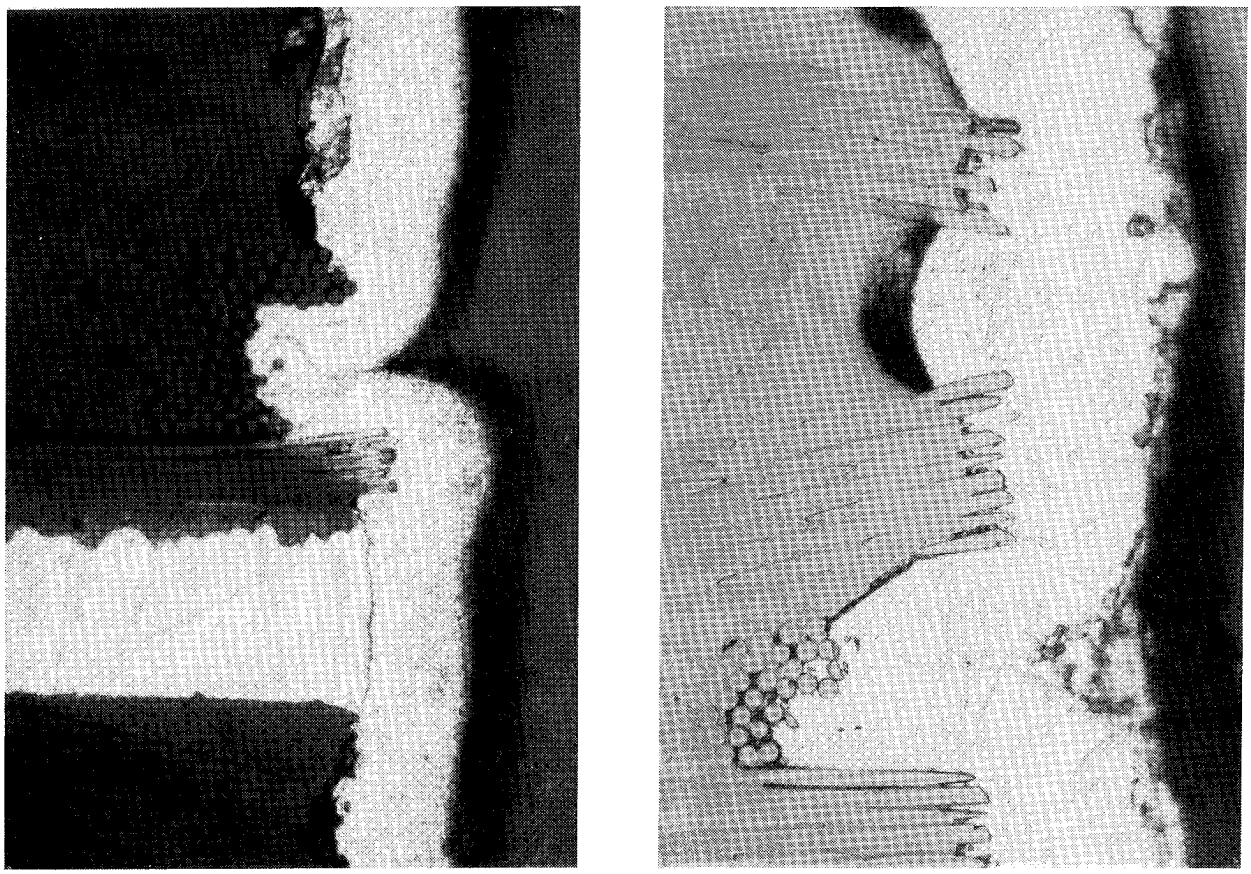


Figure 11. Plating folds resulting from irregular hole wall surface. Plating in right hand photo has columnar microstructure and should be carefully examined for cracks, particularly after solder float testing. The folds are acceptable. Etched, 400X.

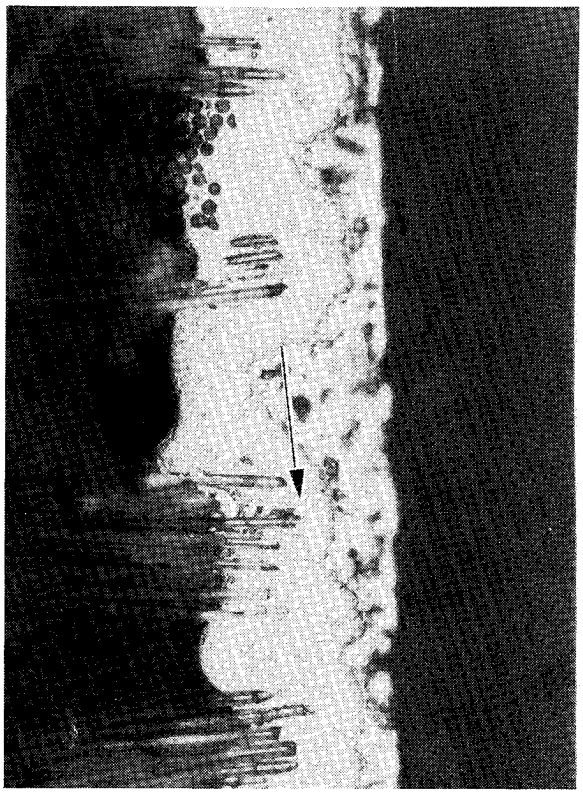
5% of the hole wall length; and the combined area of voids must not exceed 5% of the hole wall length; and the combined area of voids must not exceed 10% of the total barrel surface. (This latter measurement must be determined by visual examination of the hole wall.)

Plating voids on both sides of a hole, Figure 18a, imply potential circumferential separation, with consequent open circuits. Isolated voids, Figure 18b, probably represent round, localized gas bubbles, and are permitted if they meet the criteria listed above. Some plating voids reflect problems with the laminate and not with the actual plating process itself. The delamination at the innerplane/laminate interface illustrated in Figure 18c has caused a discontinuity, probably circumferential, in the barrel plating. The cause for rejection of this coupon might be listed as plating voids in the same plane or at a conductor interface, but corrective action should be directed toward the lamination process.

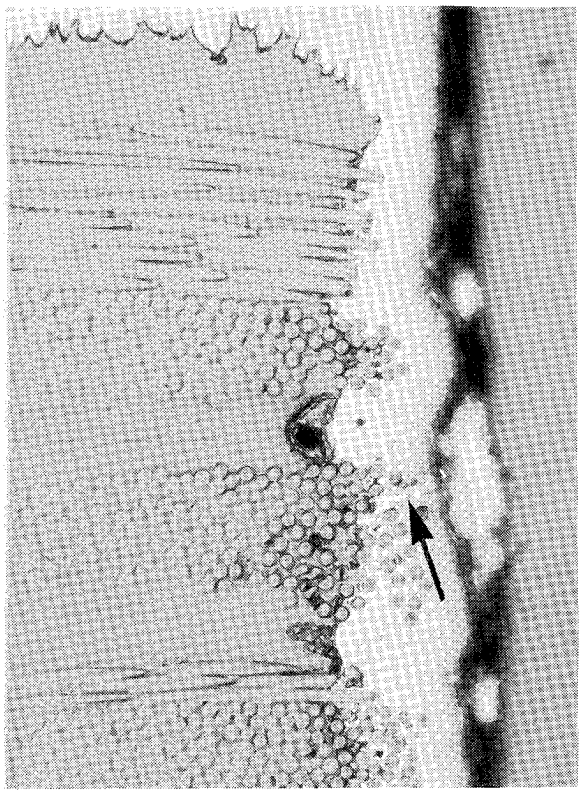
Test: Conductor Thickness
Requirement: As specified on master drawing
Method: Measured on the microsection at 100X. Copper foil thicknesses are often referred to as "one ounce," "two ounce," etc. This refers to the weight of the foil per square foot, and is the unit used by the manufacturers of clad laminate to designate foil thickness. Each ounce of copper measures 0.0014 inch.

Test: Etchback or smear removal (3.8.5, 4.8.5.5)
Requirement: a) Smear removal: PTH free of resin smear; 0.001" maximum removal of hole wall material; negative etchback 0.0005" maximum acceptable if specimen passes thermal stress (3.9.1)

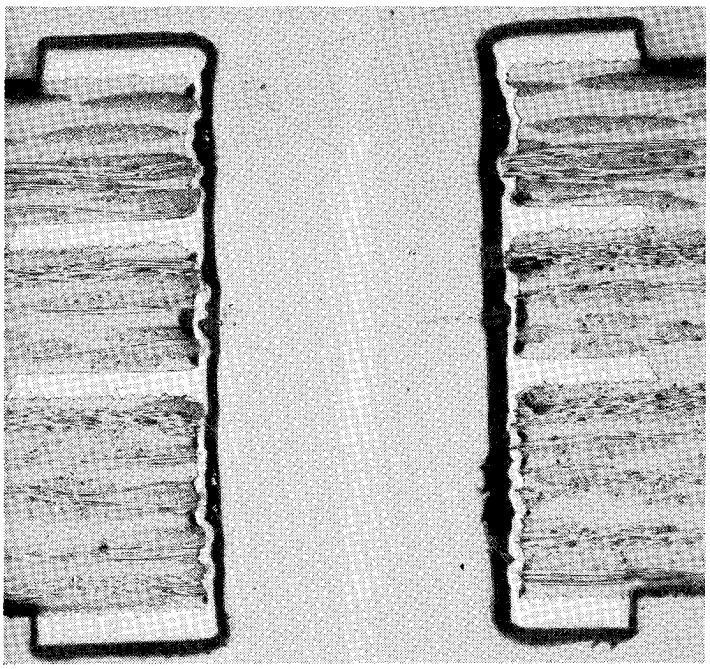
b) Etchback: (Figure A-6) PTH free of resin smear; 0.0002" minimum, 0.003" maximum (0.0005" preferred); no negative etchback; shadowing on external conductor only; additional 0.003" wicking allowed.
Method: Measured on microsection at 100X. Again, the master drawing is required to determine whether or not etchback was specified. Etchback and smear removal are both chemical treatments to clean the hole prior to plating. Smear removal cleans the epoxy from the ends of the



400X. ETCHED



400X, ETCHED, GOLD COATED



50X, ETCHED, GOLD COATED

Figure 12. Plated glass fiber protrusion is unacceptable if it reduces the copper plating thickness below the required minimum of 0.001". Cracks have also formed (arrows) in some areas of thin plating.

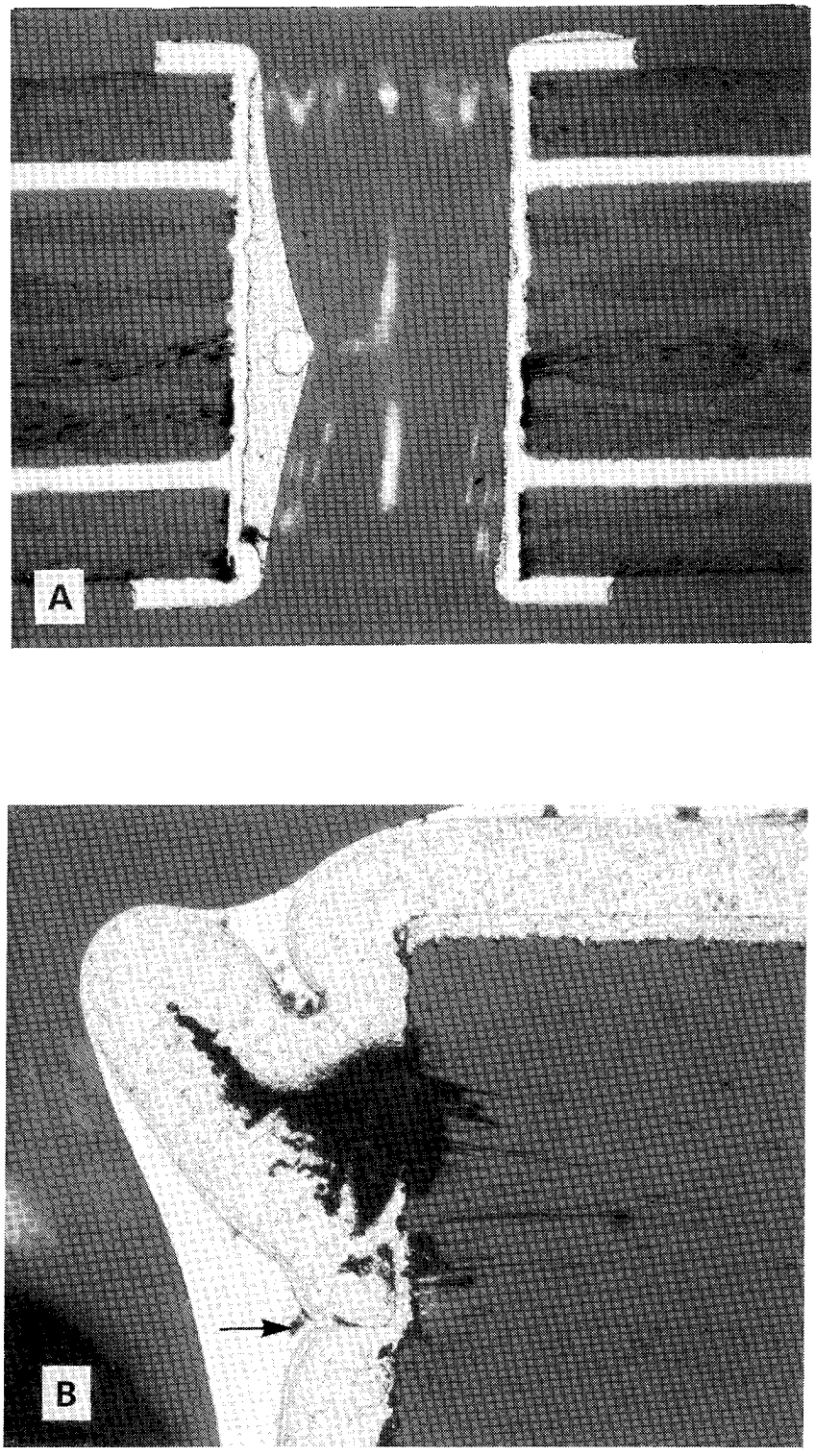


Figure 13. Nodules or plating folds that project into the hole are acceptable if they do not reduce the hole diameter below the minimum required by the master drawing. Note also the plating void. Top – unetched, 50X. Bottom – etched, 200X.

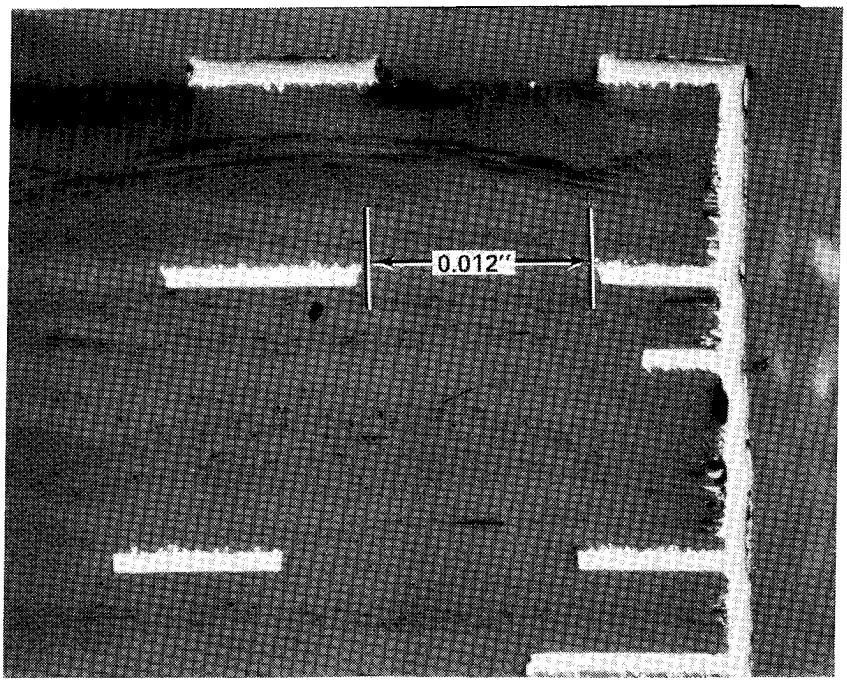


Figure 14. The minimum lateral distance from thermal planes to any conductor such as plated-through hole internal lands is 0.004", measured at the closest spacing. Unetched, 100X.

innerplanes; etchback solutions attack the glass fibers as well as the resin. Different acceptance criteria are defined for the two procedures.

An etched back hole should have the laminate slightly recessed with respect to the inner foil ends. It is difficult to control the relative removal rates of epoxy and glass, as well as the total amount of etchback, and many manufacturers do not use etchback techniques to clean the holes prior to plating. When properly done, etchback is very effective, because it cleans the foil ends and also provides a mechanical interlock between the internal conductors and the barrel plating. Too much etchback makes the hole surface irregular and hard to plate well, because of the plating folds which can result from the deeply recessed laminate between the innerplanes. Acceptable holes with varying degrees of etchback are presented in Figure 19. Negative etchback, Figure 19a, means that the ends of the copper innerplanes are recessed with respect to the laminate. This condition is acceptable within limits if etchback has not been specified, and if the specimen passes the solder float test, but is not permitted if etchback has been called out. Shadowing, Figure 20, is a form of etchback where the resin persists out to the end of the conductor even though it has been removed between the foil layers. If etchback is specified, it must be effective on at least one surface of each internal conductor. Etchback is best measured on an etched microsection, Figure 21.

Test: Undercutting (3.8.6, 4.8.5.6)
Requirement: No more than the total thickness of clad and plated copper, or 10% of the conductor width, whichever is smaller.
Method: Measured at 100X on the microsection. Undercutting is a decrease in conductor width caused by etching processes during board fabrication. It is illustrated in Figure 22.

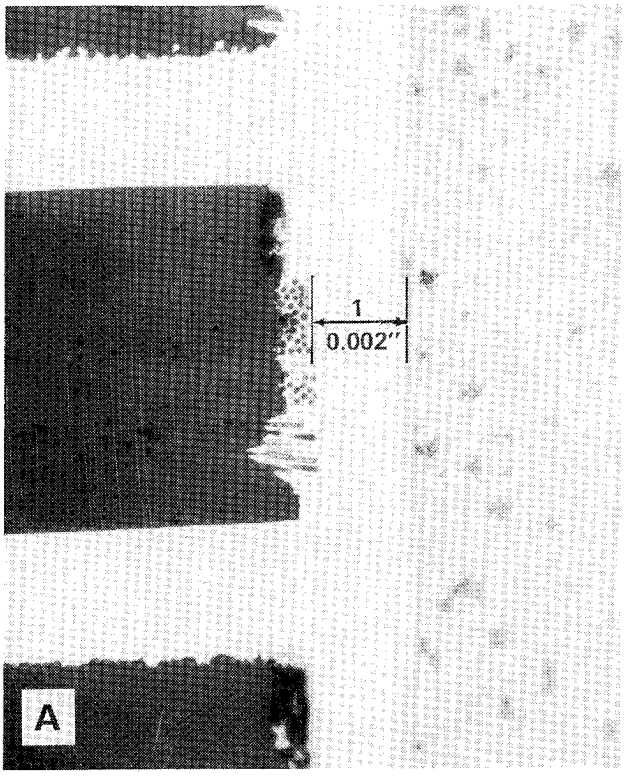
Test: Annular ring (internal) (3.8.7, 4.8.4.7, Figure A-1)
Requirement: 0.002" minimum
Method: Measured on the microsection at 100X. This measurement applies to all internal lands, both sides of the hole, for all three holes. As in the case of etchback, this measurement requires that the location of the ends of the innerplanes be defined by etching the specimen before it can be accurately carried out, Figure 23.

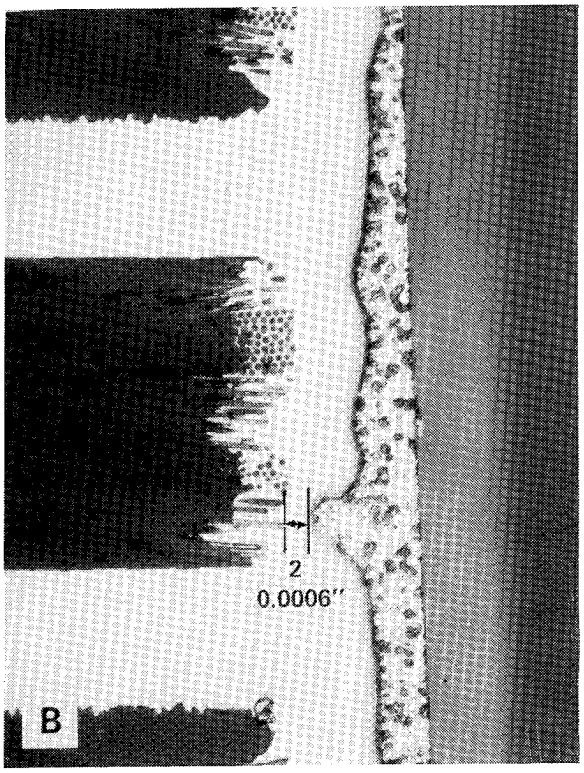
Test: Dielectric layer thickness (3.8.8, 4.8.5.8, Fig. A-7)
Requirement: Types 1, 2 and 3: As specified on the master drawing, 0.0035" minimum on finished Type 3 boards.
Method: Measured at 100X on the microsection. The measurement for the 0.0035" minimum is made at the location of the closest spacing between copper foil layers; all other measurements shall be made at the maximum point of dielectric thickness.

A. MEASURE AT THREE TYPICAL LOCATIONS, SUCH AS AT 1, AND AVERAGE THE MEASUREMENTS.

B. ISOLATED THIN SPOTS MEASURING LESS THAN 0.0008", AS AT 2, ARE TREATED AS PLATING VOIDS.

C. REJECT IF AVERAGE THICKNESS IS LESS THAN 0.001".





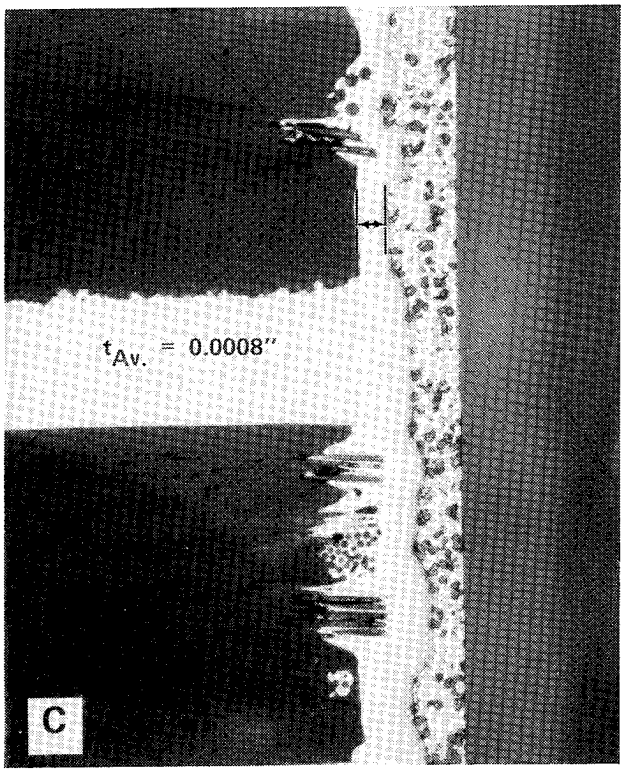
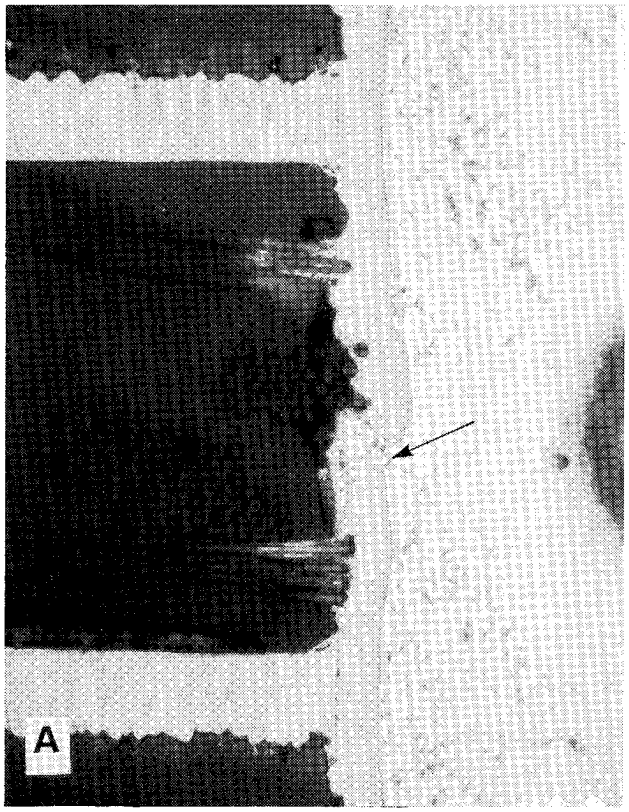


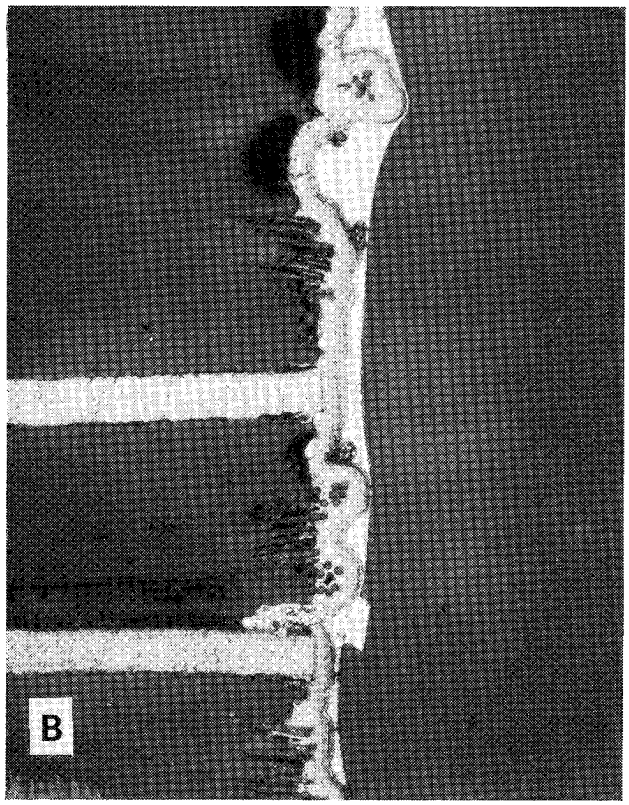
Figure 15. Copper plating thickness measurement. Unetched, 200X.



A. PLATING WHICH IS TOO THIN (IN THIS CASE, 0.0005") CAN CRACK UNDER THERMAL STRESS. ETCHED, 400X

B. THIN PLATING IF OFTEN ASSOCIATED WITH POORLY DRILLED, RAGGED HOLES, NODULES, AND PLATING VOIDS. ETCHED, 200X.

C. AS B, BUT UNETCHED.



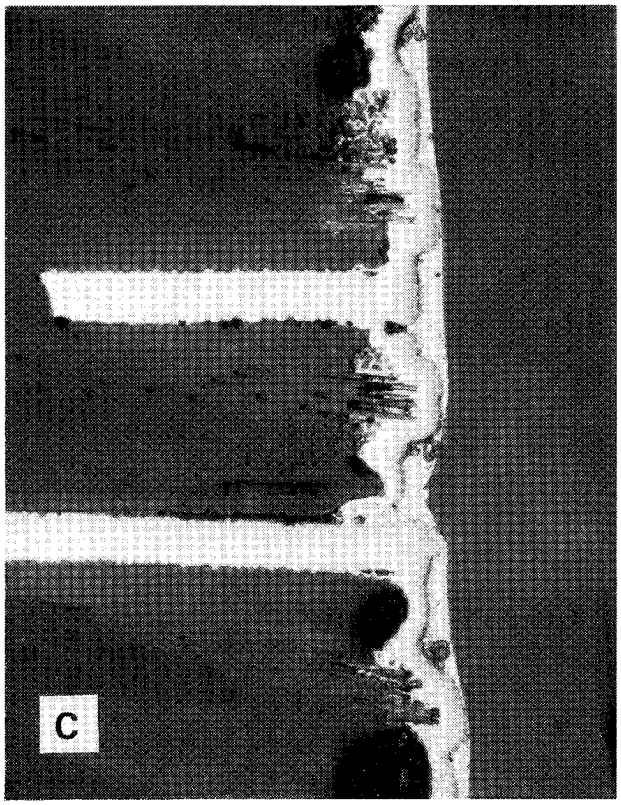
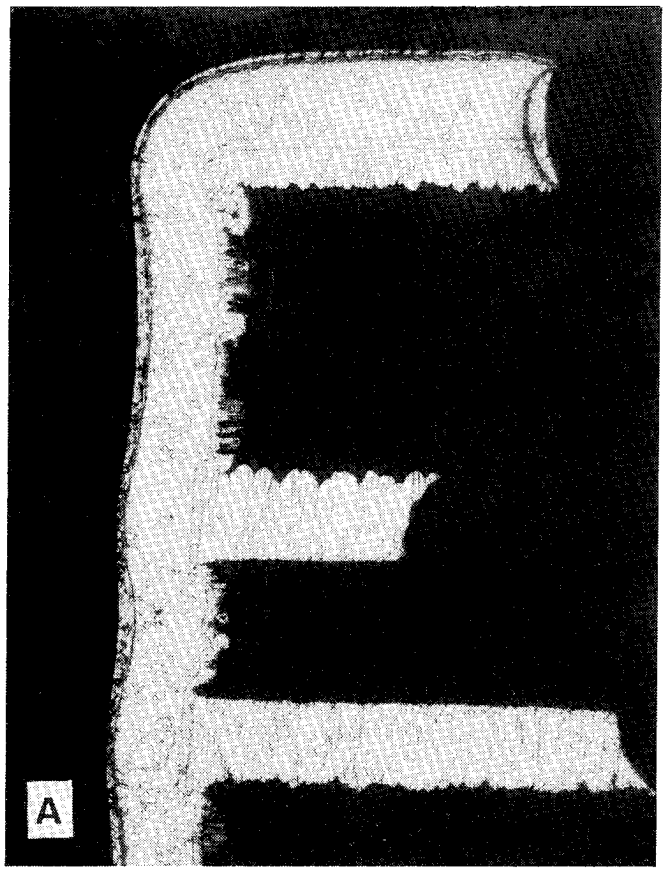


Figure 16. Examples of inadequate barrel plating.

A. DESIRABLE PLATING MICRO-STRUCTURE IS FINE-GRAINED AND EQUI-AXED; IT IS GENERALLY DUCTILE AND RESISTS GRAIN BOUNDARY CRACKING.

COLUMNAR MICROSTRUCTURE OF INNERPLANE FOIL LAYER IS NORMAL.

ETCHED, 175X.



B. MORE THAN ONE LAYER OF BARREL PLATING MAY BE PRESENT. NAIL-HEADING IS WITHIN ACCEPTABLE LIMITS (1.2). ETCHED, 500X.

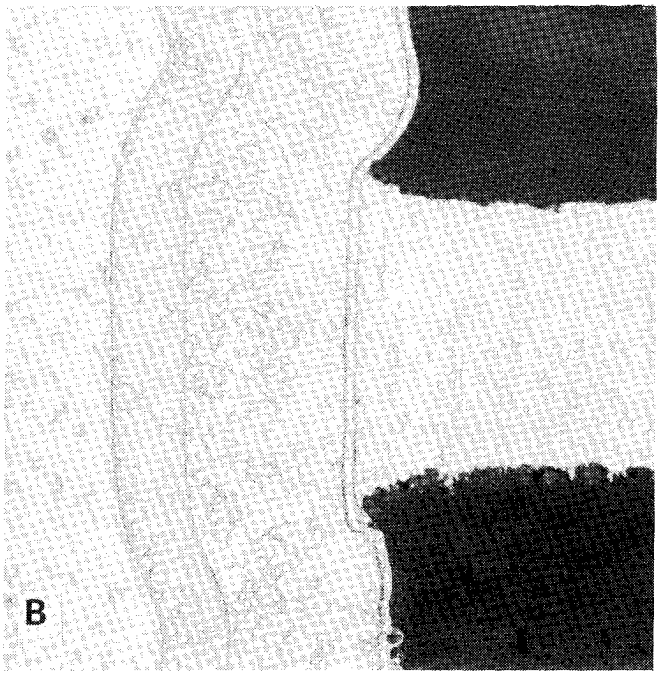
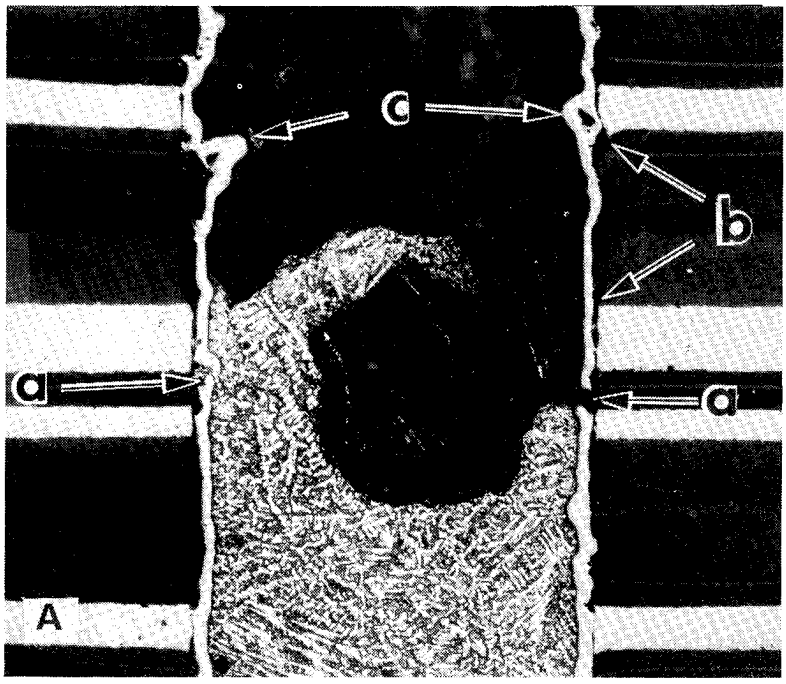


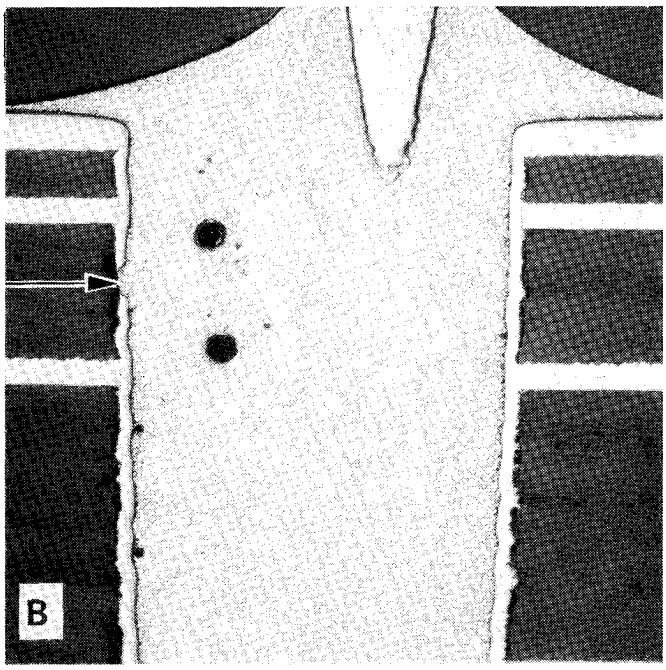
Figure 17. Examples of acceptable hole plating. Thickness in both cases is adequate and no defects are noted.

A. PLATING VOIDS IN THE SAME PLANE (a–a) ARE FORBIDDEN. NOTE ALSO SEPARATIONS (b) AND PLATING NODULES (c). UNETCHED, 80X.

B. ISOLATED PLATING VOIDS (ARROW) ARE ACCEPTABLE IF NO MORE THAN THREE PRESENT IN ONE HOLE. UNETCHED, 50X.

C. PLATING VOID RESULTING FROM NON-BRIDGING OF DELAMINATION. SOLDER HAS WICKED INTO DELAMINATION DURING REFLOW. ETCHED, 200X.





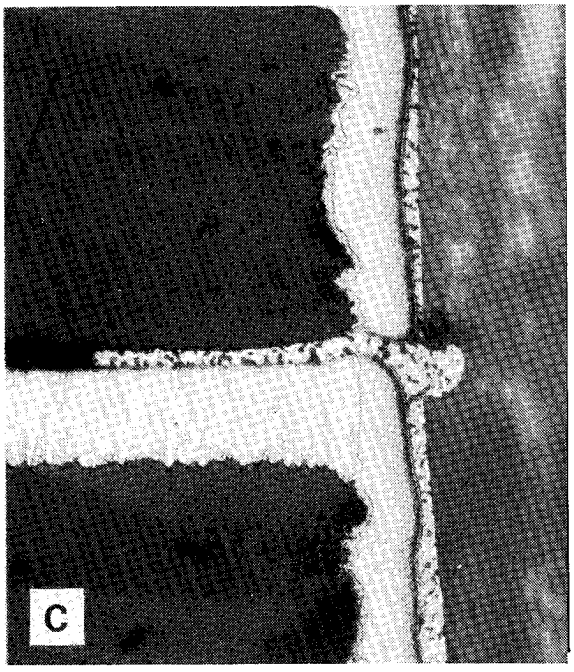


Figure 18. Examples of plating voids. The coupon illustrated in A should be rejected for plating voids and separations; that in B is acceptable for plating voids but has rejectable separations; C is rejectable for delaminations.

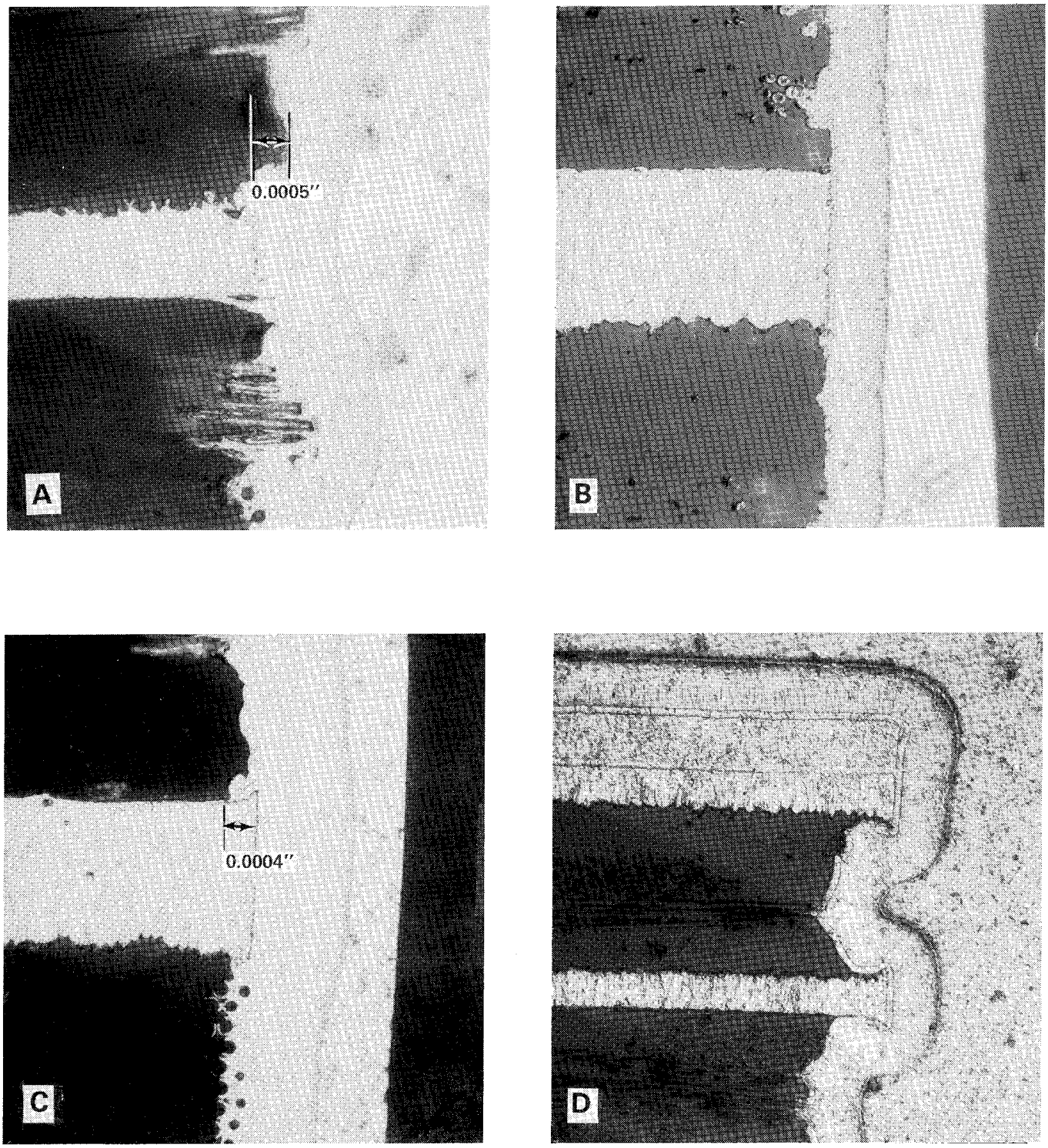
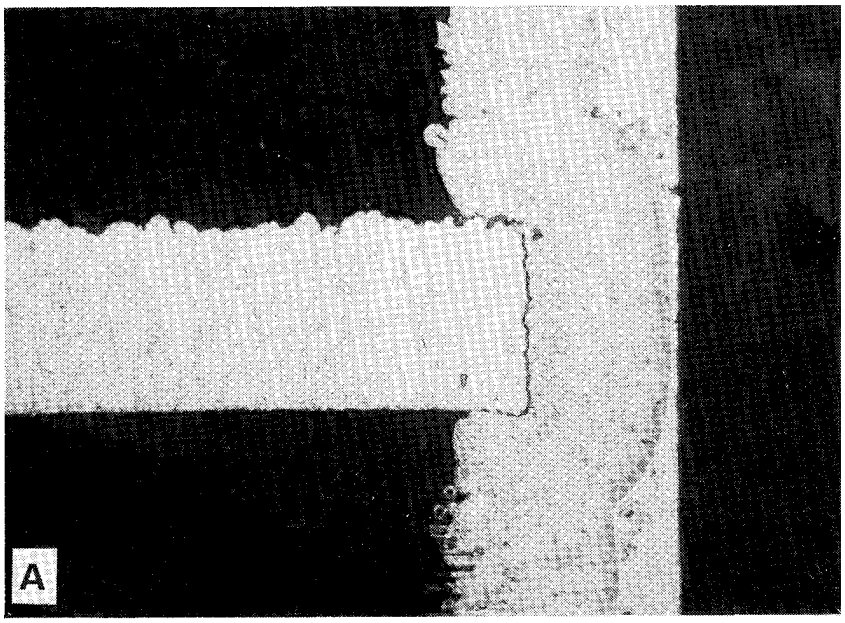
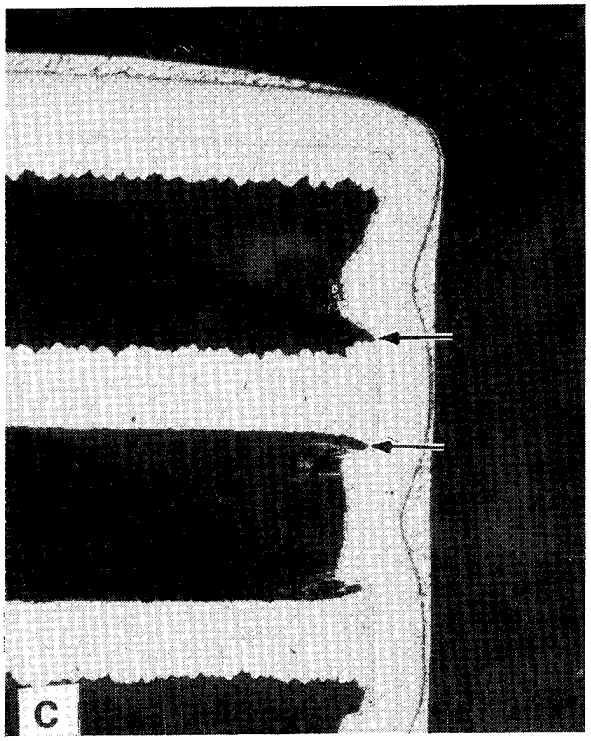


Figure 19. Forms of etchback. Holes in A and B were cleaned by smear removal, those in C and D by etchback. All are acceptable, although A and B would not be had etchback been specified. A = negative etchback; B = no etchback; C = etchback of 0.0004"; D = etchback of 0.002". Magnification: A – 500X, B and C – 400X, D – 200 X. Etched.



A. ETCHBACK EFFECTIVE ON BOTH SIDES OF INTERNAL CONDUCTOR. ETCHED, 400X.

B. ETCHBACK EFFECTIVE ON ONE SIDE. ETCHED, 400X.



C. SHADOWING ON BOTH SIDES. ETCHED, 200X.

Figure 20. Etchback should be effective on at least one side of each internal conductor.

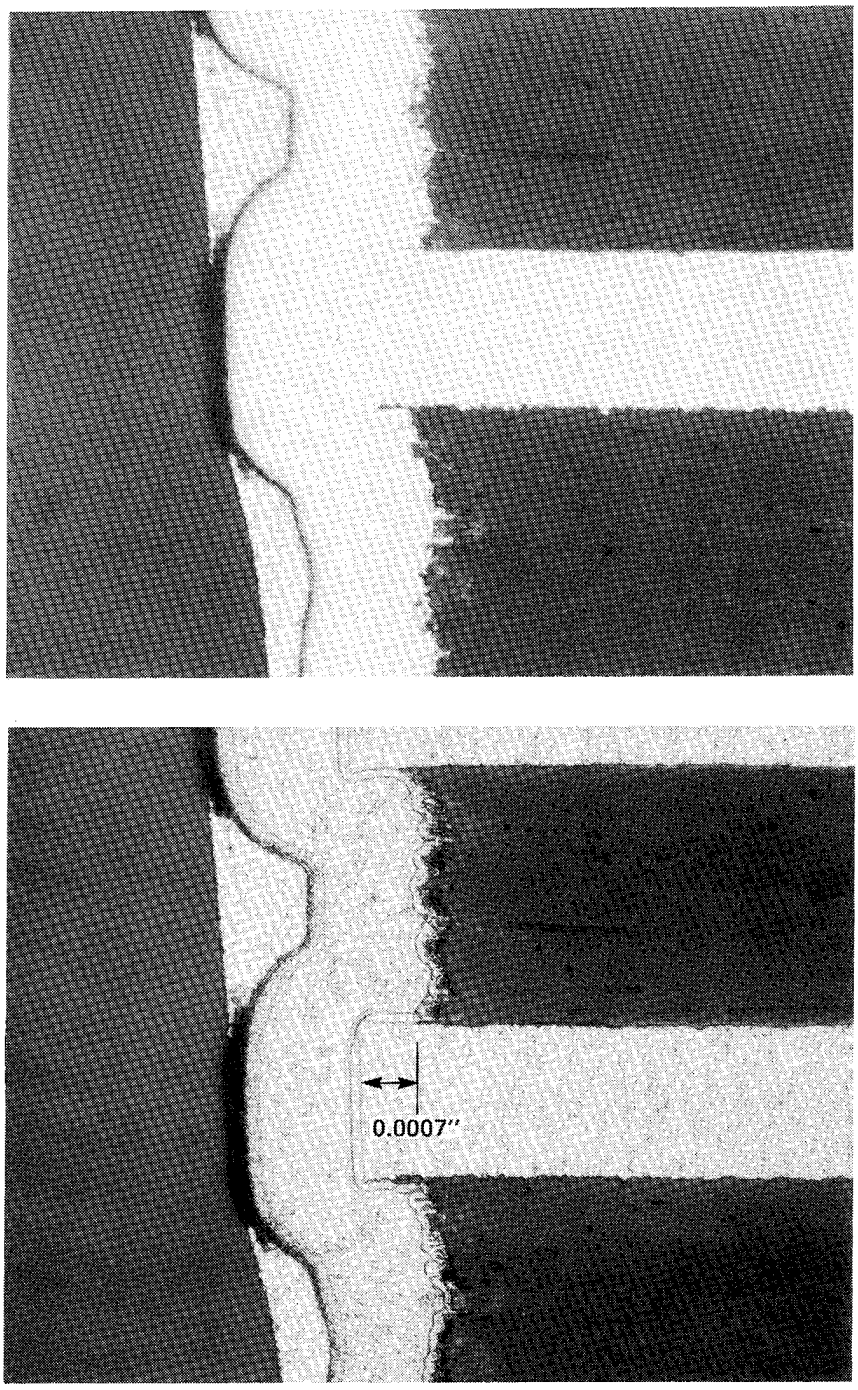


Figure 21. Etchback cannot be measured accurately on an unetched microsection. Unetched (top) and etched (bottom) at 400 X.

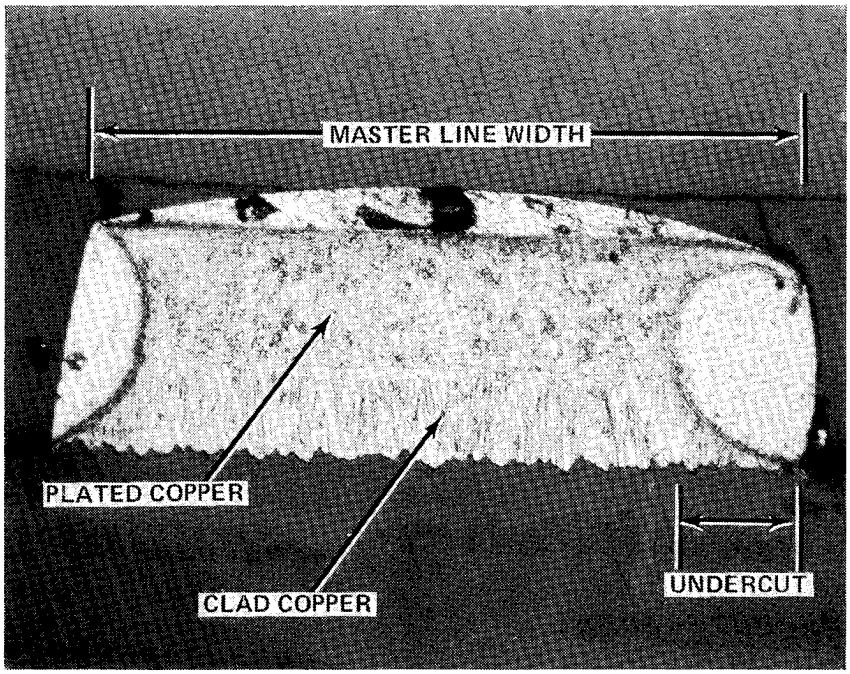


Figure 22. Undercutting must be less than the total thickness of clad and plated copper, or 10% of the conductor width, whichever is less.

Test: Laminate voids (3.8.9, 4.8.5.9)
Requirement: 0.003" maximum (in longest dimension)
Method: Measured on the microsection at 100X. Laminate voids can occur within the laminate itself, Figure 24a, or at the interface between the laminate and a conductor, Figure 24b. They may result from poor quality laminate or B-stage, poor laminating procedures, or be caused by outgassing of the resin at high temperatures such as are encountered during fusing, solder reflow, solder float or rework simulation testing. A delamination is a planar laminate void usually at a laminate-laminate or laminate-conductor interface. For microsection examination, a delamination is counted as a laminate void.

The hole illustrated in Figure 24a is shown at higher magnification in Figures 25a - 25c. This hole had not been solder float tested. Faulty lamination procedure has resulted not only in voids or warpage, but has squeezed almost all the resin out of the B-stage spacer (resin starvation), to the point of breaking some glass fibers, and decreasing the dielectric thickness between the conductive layers to an unacceptable degree.

Test: Resin recession (3.8.10, 4.8.5.10, Fig. A-8)
Requirement: 0.003" maximum from hole surface; < 40% of the total dielectric thickness
Method: Measured on microsection at 100X. Resin recession takes the form of half-moon shaped voids behind the barrel plating, Figure 26. It is caused by thermally induced degradation of the epoxy resin, typically during solder reflow, fusing, or thermal stress testing. The resin recession seen in Figure 26b exceeds the permissible limits for a hole which has not been solder float tested.

Test: Lifted lands (prior to stress) (3.8.11, 4.8.5.11)
Requirement: None permitted
Method: Evaluated on the microsection at 100X. The external annular ring (land) must not be lifted from the laminate surface on an as-received specimen. This test is made after solder reflow or fusing, but before thermal stress testing.

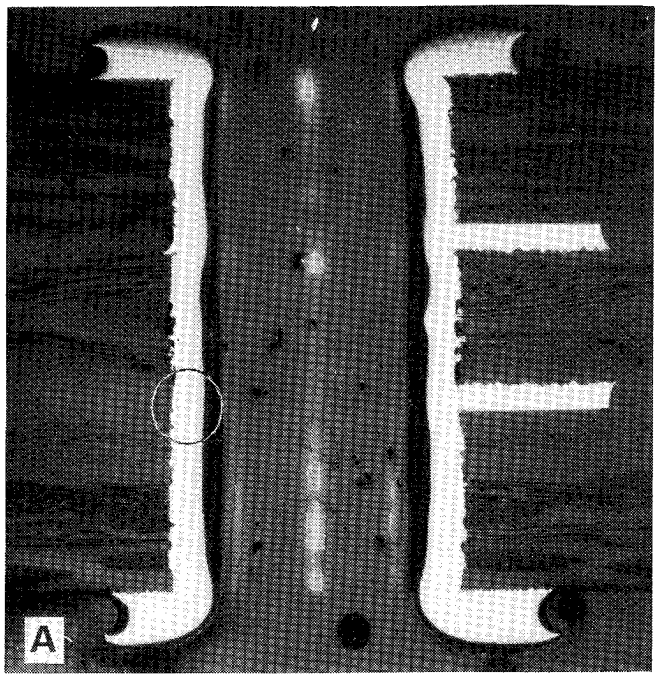
Test: Plated-through holes after stress (3.9.1, 4.8.6, Fig. A-8)
Requirement: As for unstressed PTHs except as described below
Method: Examination of three solder-float tested holes in vertical microsection at 100X (referee magnification 200X)

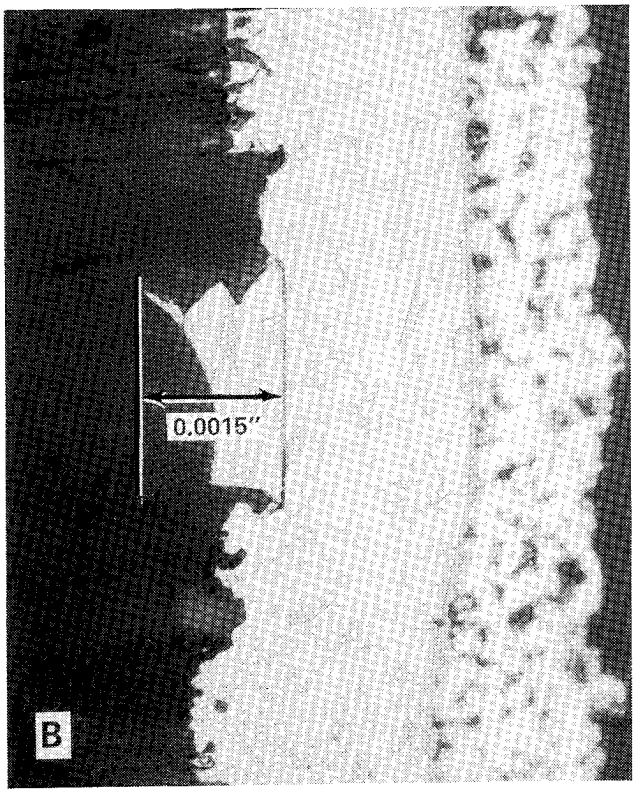
Different evaluation criteria for laminate integrity are applied to as-received and thermally stressed (solder float tested) coupons. The rationale is that some degradation of the epoxy/glass laminate is virtually inevitable from the heat associated with the solder float test, and requirements for freedom from voids and resin recession should be relaxed in the immediate area of the plated-through hole after thermal stressing. The as-received specimen is evaluated as a unit, but the required three-hole cross-section of the thermally stressed coupon will have three "Zone A" areas for plating evaluation, consisting of the holes them-

A. POOR REGISTRATION OF INTERNAL LAYERS HAS RESULTED IN ALMOST NO ANNULAR RING ON ONE SIDE OF THE HOLE. UNETCHED, 50X.

B. AREA CIRCLED IN A, ETCHED, 500X. ANNULAR RING IS BELOW MINIMUM OF 0.002"

C. ANNULAR RING BARELY MEETS MINIMUM. ETCHED, 400X.





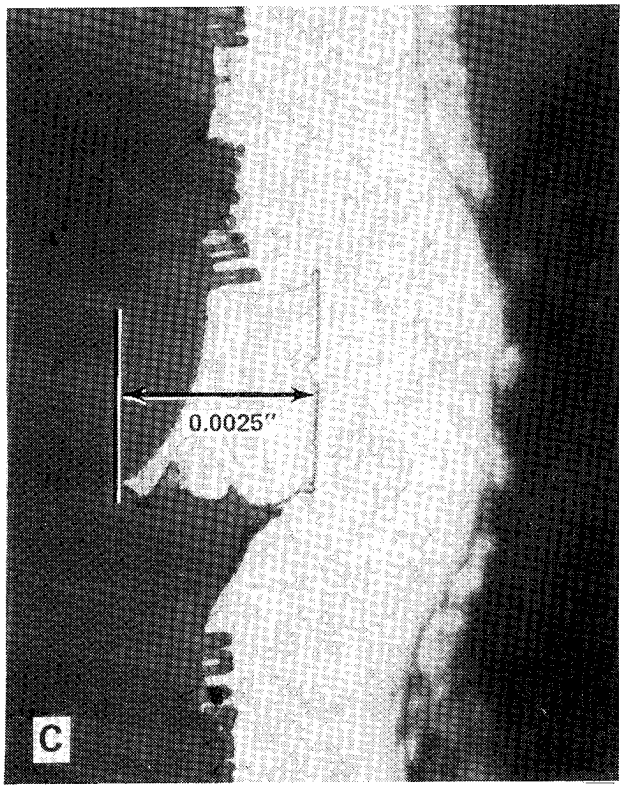


Figure 23. Internal annular ring should measure 0.002" minimum. Measurement should be made on etched specimen at 100 – 200X.

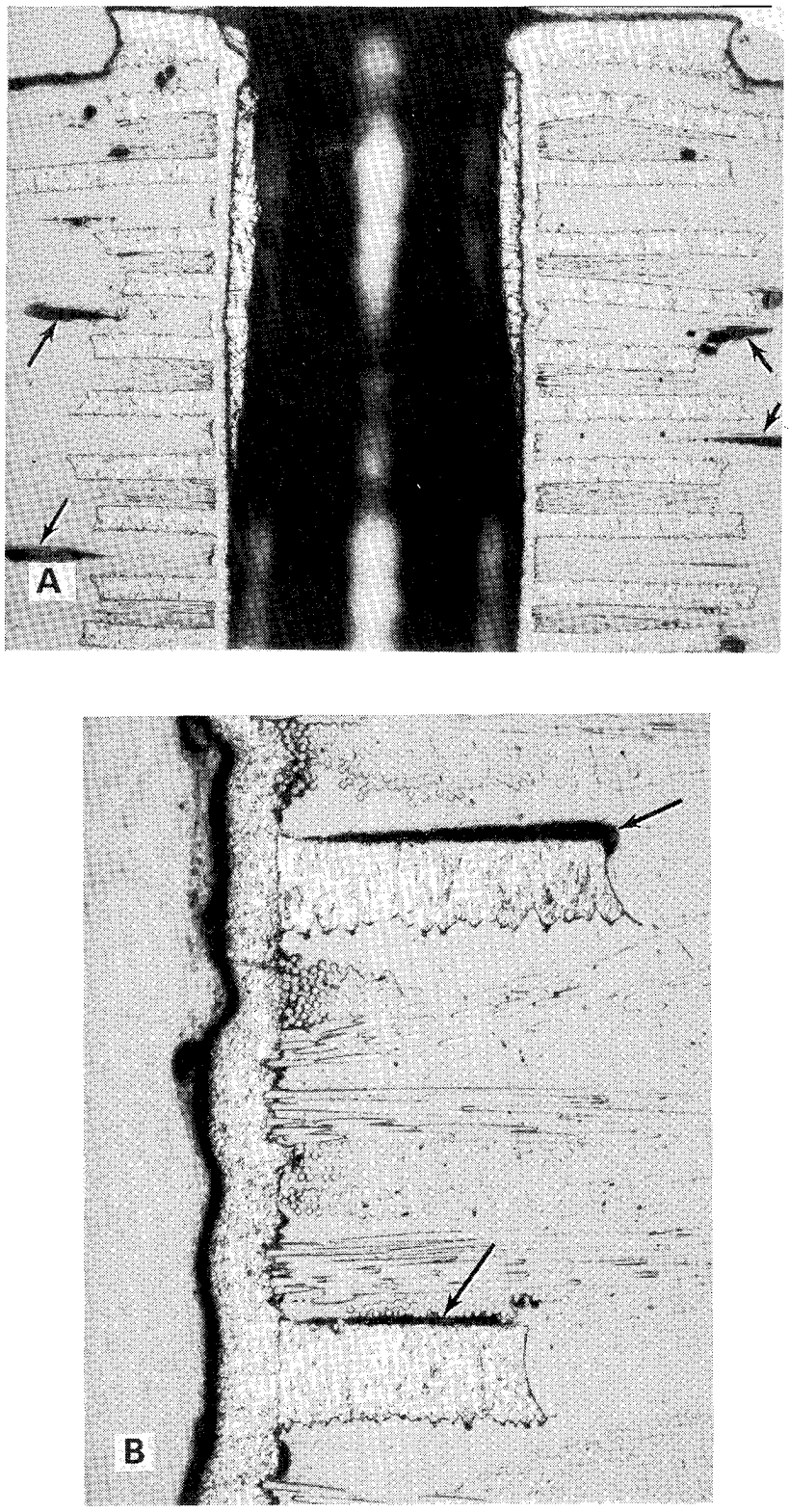


Figure 24. Laminate voids greater than 0.003" are grounds for rejection. Voiding in A is a result of poor laminating procedures. Voids at conductor/laminate interfaces in B are also rejectable in an unstressed (not solder float tested) specimen.

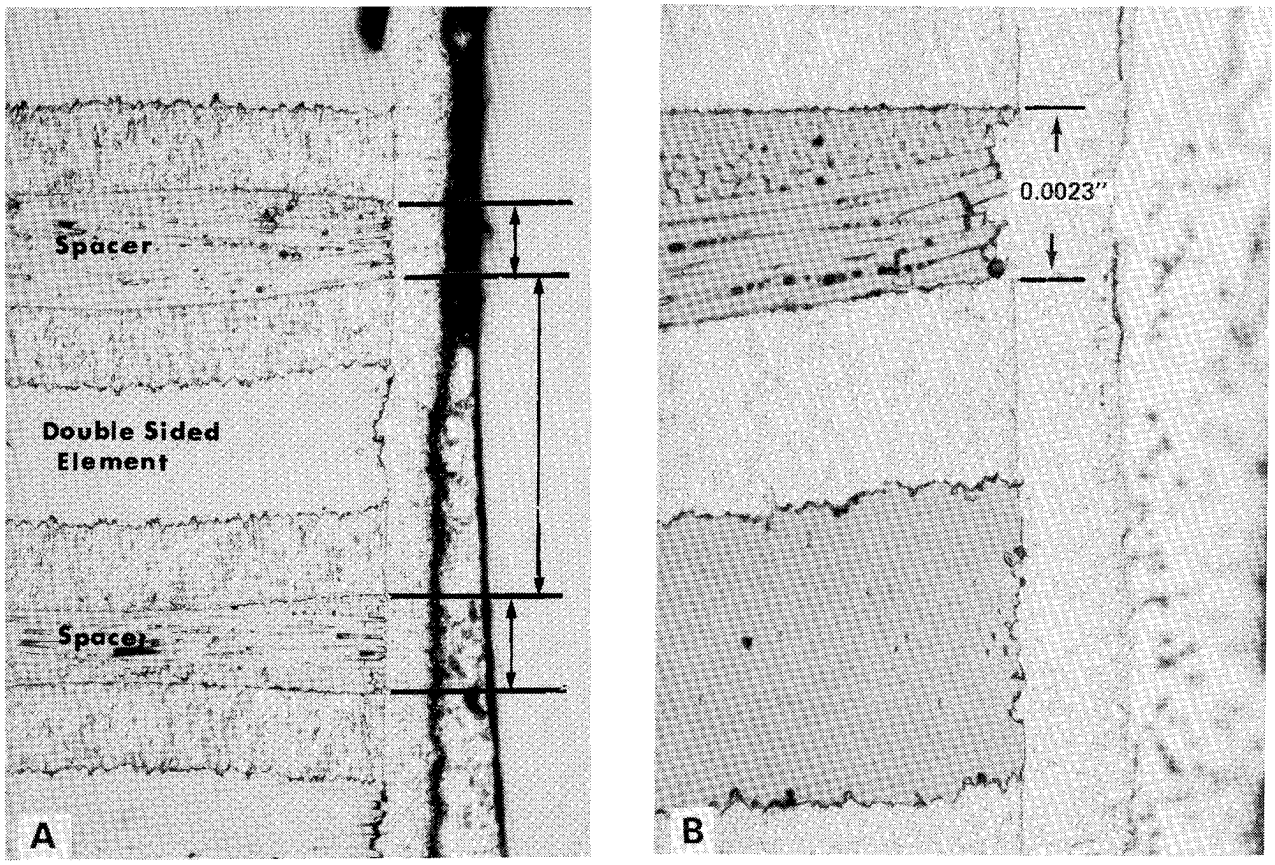


Figure 25. Faulty lamination has squeezed most of the resin out of the B-stage spacers (resin starvation), causing the dielectric thickness between adjacent layers to be reduced below the permissible minimum of 0.0035". A – Etched, 175X. B – Etched, 400X.

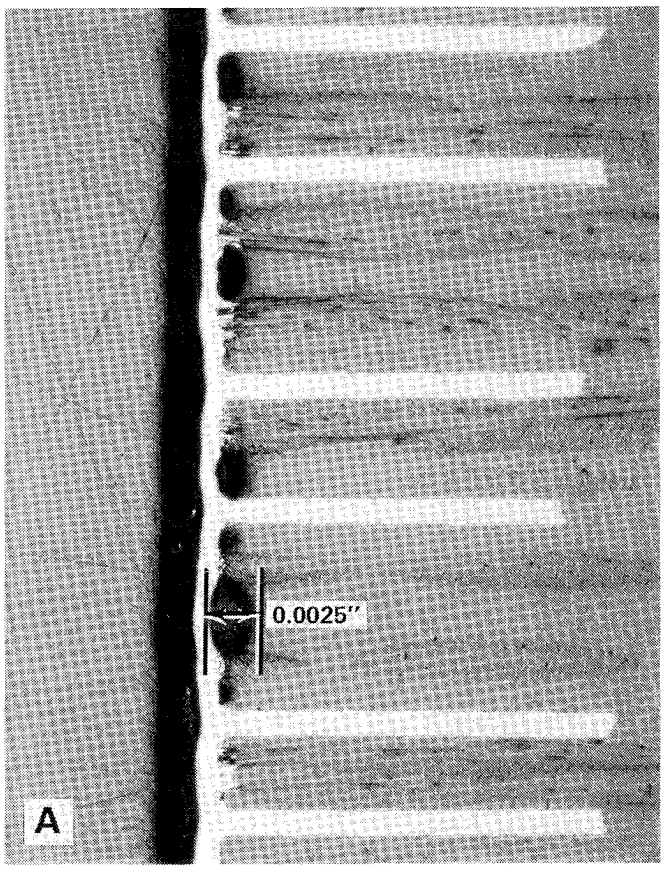
selves plus a maximum of 0.003" of the laminate beyond the lands associated with the hole; and two "Zone B" areas, consisting of the areas between the Zone A areas, that is, the spaces between the holes, which are used for laminate evaluation. The laminate is not evaluated in Zone A for a solder-float tested coupon.

For the entire as-received coupon and for the Zone B areas of solder-float tested coupons, the maximum permitted laminate void has a longest dimension of 0.003 inch. Laminate voids are not evaluated in Zone A of solder-floated coupons, but voids greater than 0.003" extending from Zone A into Zone B are grounds for rejection, Figure 27.

As for the unstressed specimen, cracks in the internal conductive foils, platings or coatings are forbidden. After thermal stress, however, cracks in the outer copper foil are permissible provided they do not extend into the plated copper, see Figure 28. Measling in solder float tested specimens may not exceed that of IPC-A-600, class 3 [see 4.8.6, page A-5]. Measles, Figure 29, are visible on the surface of the board or coupon as squarish white spots, and are splits between two bundles of glass fibers where they cross each other in the weave of the glass cloth. They occur typically just under the surface in the land area. In cross section, measles appear as voids. Blisters are localized swellings on the surface of the board. The IPC measling requirement is accomplished by visual inspection of the production board.

Test: Lifted lands (after thermal stress) (3.9.4, 4.8.6.4)
Requirement: 0.003" maximum lift; 50% of land bonded to each side of hole (Fig. A-9)
Method: Measured on solder float tested microsection at 100X. Figure 30a illustrates lifted lands just barely meeting the 50% bond criterion. Figure 30b shows a PTH with excessive lifted lands and measles. This coupon had been submitted for evaluation with terminals already soldered into some of the holes.

A. RESIN RECESSION MAY NOT EXCEED 0.003" BEHIND THE BARREL PLATING. UNETCHED, 100X.



B. RESIN RECESSION IN THIS HOLE EXCEEDS THE MAXIMUM PERMISSIBLE AMOUNT OF 40% OF THE TOTAL DIELECTRIC THICKNESS. ETCHED, 50X.

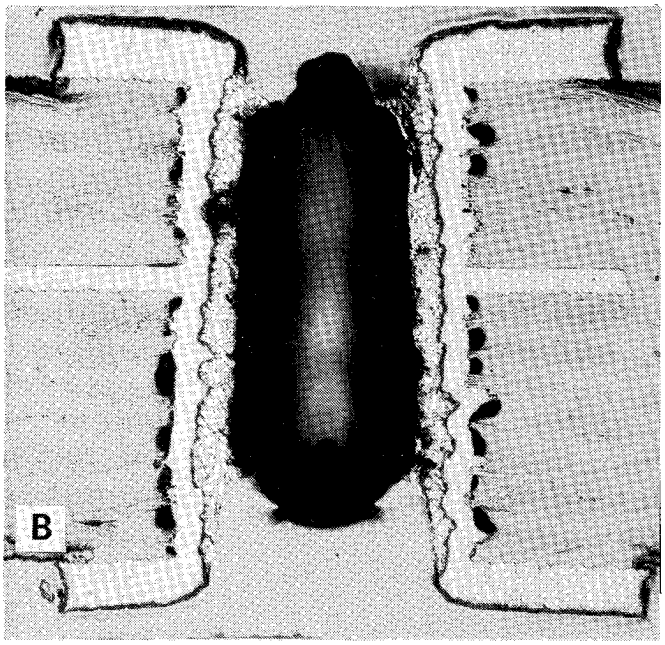


Figure 26. Examples of resin recession.

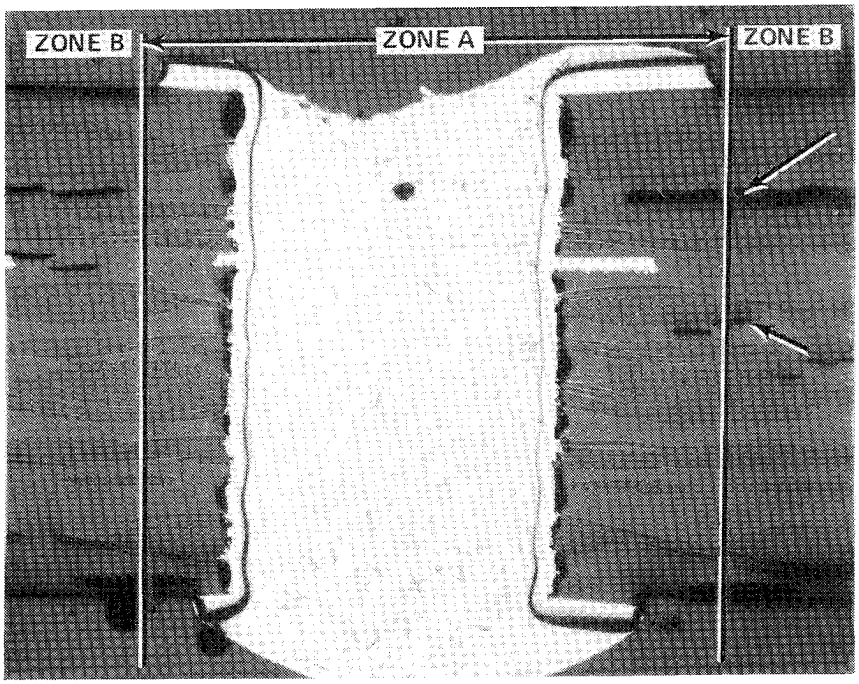


Figure 27. After solder float testing, the laminate is not evaluated in Zone A, that is, resin recession and laminate voids are acceptable in this "thermal zone." Voids in Zone B are evaluated to the same standards set forth for as-received specimens. Voids greater than 0.003" which extend from Zone A into Zone B (arrows) are grounds for rejection. 50 X.

The portion of Group B testing that is of concern to the metallographer is the plated hole examination (3.9.2) after rework simulation (4.8.6.2). This test is described in IPC-TM-650, Test Method 2.4.36, and calls for soldering and unsoldering wires into plated through holes five times. After the fifth cycle, the holes are microsectioned and examined for defects. The examination is similar to that following the thermal stress test of Group A testing.

Beyond MIL-P-55110:

Paragraph 4.8.1.2 states that microsectioning should be done using methods in accordance with IPC-TM-650, Method 2.1.1. This specification outlines a procedure for specimen preparation, but is not primarily concerned with examination procedures. Aside from directing that plating thickness be measured at a minimum magnification of 100X, the only reference to multilayer board inspection is "plating quality . . . may include innerplane bond to plated-through hole, resin smear, glass fiber protrusion, and epoxy etchback. Some of these conditions may be observed on the polished specimen prior to etching." MIL-P-55110D specifies that foil and plating integrity be examined at 100X, with referee examinations performed at 200X, but makes no mention of etching the specimen.

For most of the defects illustrated up to this point, examination at 100X, etched or unetched, would probably be sufficient. However, for high reliability multilayer boards it is essential that the bond between the innerplanes and the barrel plating be metallurgically sound, and at 100X, particularly in the etched condition, subtle but important features of this bond may not be readily apparent. A search of this Metallography Laboratory's files, extending back some fifteen years, turned up very few photographs of etched specimens at 100X--the one in Figure 31 was taken especially for use in this document. There were many pictures of holes at 50X illustrating laminate voids, misregistration, and gross plating defects, but 200X was the preferred magnification for routine examination of plating quality and especially for looking for defects at barrel/innerplane interfaces; 400X was frequently used for clarity of illustration.

In Figure 31, it is not easy to distinguish which innerplane/barrel junctions are good and which are questionable. In Figure 32, several junctions on the same coupon (not necessarily the same hole) are shown at 200X, unetched and etched. The defects are more easily observed at the higher magnification, prior to etching. Even at 200X, a dark-etching copper strike layer may be mistaken for a separation if the junction has not been already examined before etching, as illustrated in Figure 33.

Examination prior to etching is also important for one type of defect which is not clearly defined in MIL-P-55110D: a very fine demarcation line--not a separation or

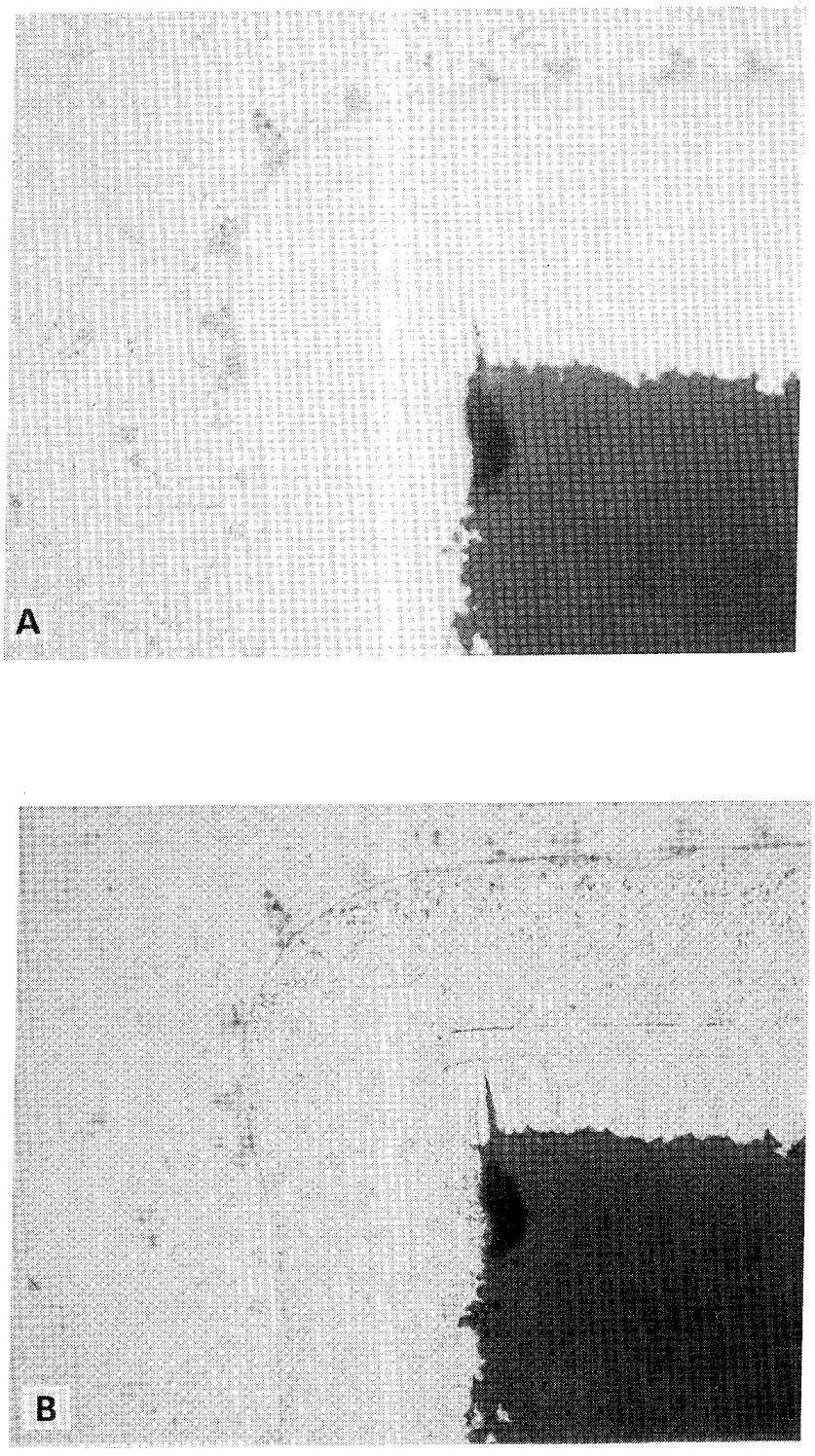
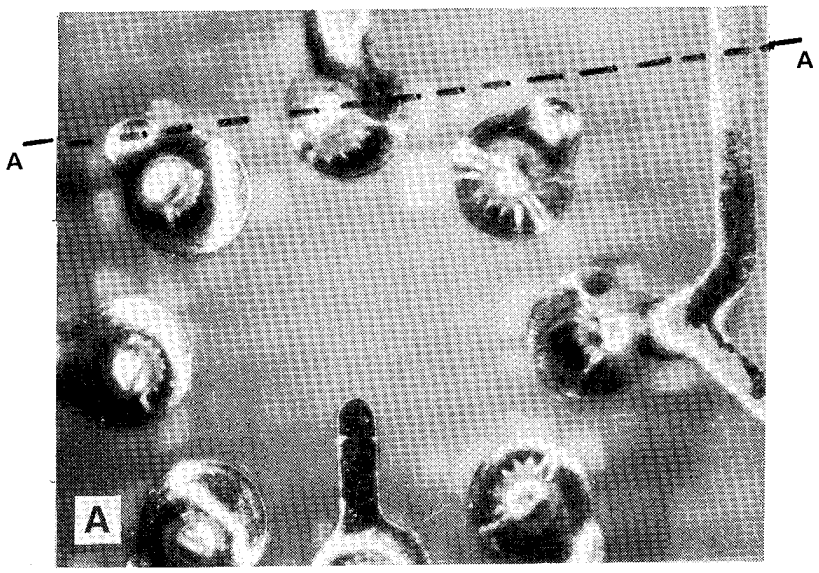


Figure 28. After solder float test, cracks in the outer surface foils are permitted provided they do not extend into the through-hole plating. Extent of cracking can only be determined after the specimen is etched. This condition is not acceptable prior to solder float. Top – Unetched, 400X; Bottom – Etched, 400X.

A. SURFACE OF BOARD SHOWING MEASLES (LIGHT SQUARISH AREAS) WHICH DEVELOPED NEAR SOLDERED HOLES. 10X.

B. CROSS-SECTION THROUGH A–A ABOVE AT 50X. MEASLES ARE SUBSURFACE SPLITS BETWEEN INTERWOVEN GLASS FIBER BUNDLES. THE SOLDER HAS ETCHED BLACK IN THIS PHOTOGRAPH.



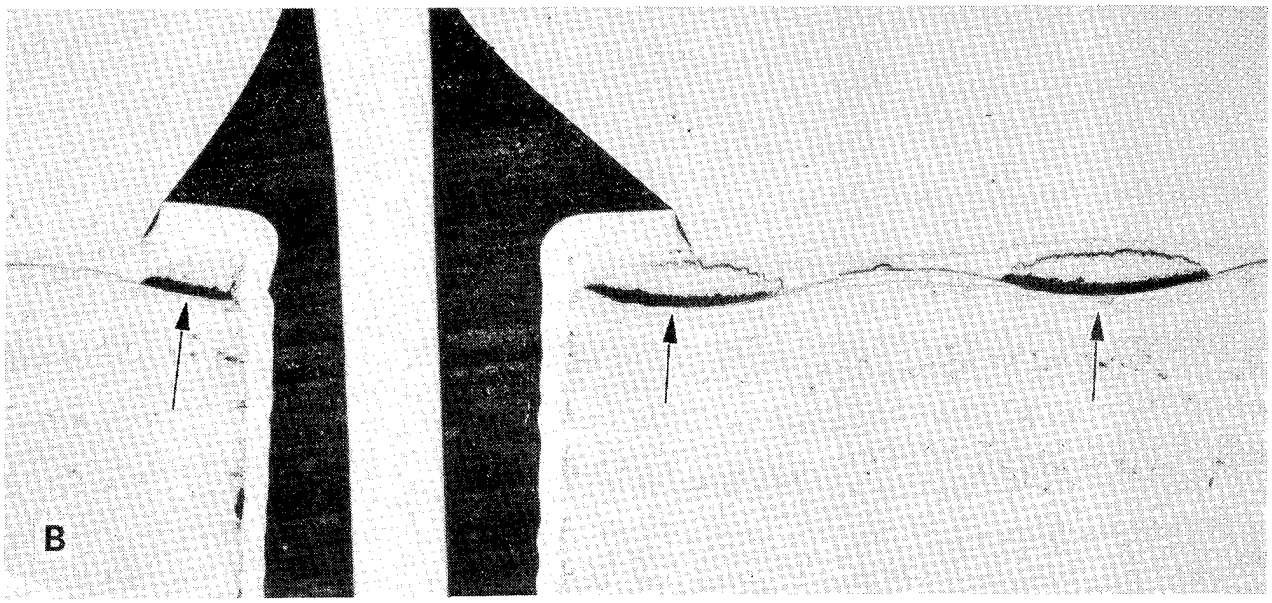


Figure 29. Measles which bridge more than 25% of the space between adjacent conductors or cover more than 1% of the board surface area are not permitted.

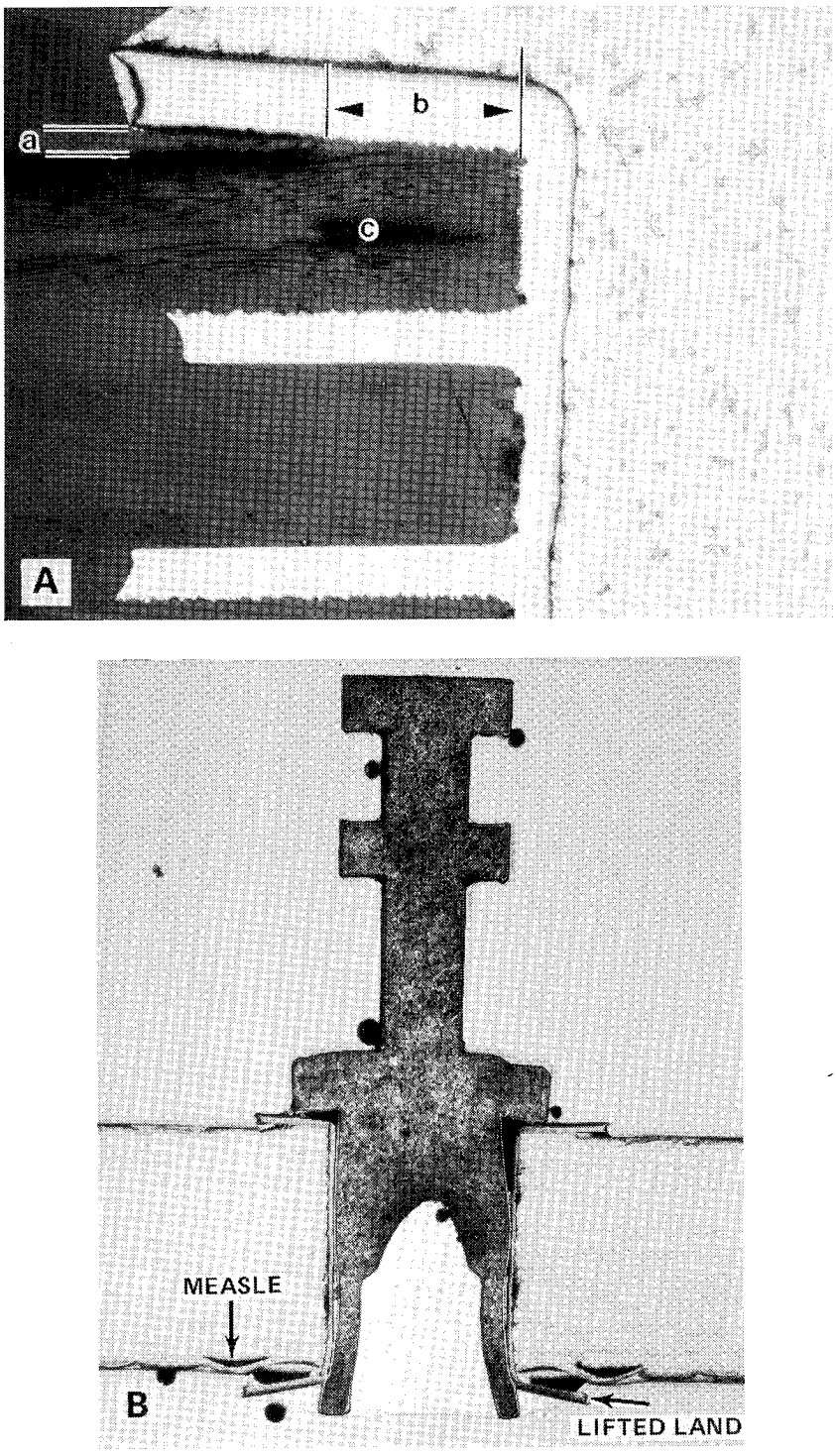


Figure 30. Lifted lands after thermal stress.

A. After solder float, lands may not be lifted more than 0.003" from the board surface (a) and must have 50% intact bond to the surface (b). Laminate voids (c) are not evaluated in Zone A. Unetched, 100X.

B. Excessive land lifting and measling on double-sided board with a soldered-in terminal. Etched, 15X.

epoxy smear—at the interface between the hole plating and the ends of the innerplanes. This condition is not infrequent, and at the GSFC Metallography Laboratory is considered a potentially serious defect. Examples are shown in Figure 34 at magnifications ranging from 200X to 500X. They are difficult to see at lower magnifications, and sometimes virtually impossible to detect if the sample has been etched.

Since the barrel plating and the foil of the innerplanes are applied to the board at different times, and are distinct entities, when the specimen is etched to reveal the microstructure of the copper there will always be a demarcation line at the interface between the drilled ends of the innerplanes and the hole plating where the grain structure of the foil, interrupted by the hole, meets, but does not match, the grain structure of the barrel plating. In the unetched condition, however, there should be *nothing* visible at this location if the bond is good.

The examples pictured in Figure 34 are from board coupons which were sectioned after an increase in resistance was traced to a plated-through hole on one of the boards (previously illustrated in Figure 8b). These coupons had not been thermally stressed (solder float tested). Fine linear features were observed at a number of the barrel/foil junctions. When a board coupon exhibiting similar "fine line defects" was sectioned before and after thermal stressing, several barrel/foil junctions had opened up, and are presumed to have had fine line defects prior to solder float testing, Figure 35. One reference (2) attributed the presence of this linear feature to large particle size in the palladium-tin catalyst which is normally used to prepare the drilled and cleaned hole to accept the initial electroless copper upon which the subsequent layer(s) of electrolytic copper are deposited. Other instances have been attributed to oxidation of the ends of the innerplanes. Whatever its origin, the presence of a visible line at the interface is judged to be detrimental by the GSFC Metallography Laboratory.

The weak junctions that open up into actual separations during solder float testing are easy to spot and the coupon would be rejected on that basis whether or not the as-received coupon showed fine line defects. However, even if such junctions do not separate after thermal stress, they may fail by thermal fatigue during thermal cycling tests or during service. The usual failure mode is an increase in resistance or a transient open at the high end of the temperature cycle. In many cases, completed assemblies are tested electrically before and after, but not monitored during, thermal cycling, so that anomalies caused by a change in temperature are not detected. It is thus important that coupons be carefully examined, preferably unetched at 200X, for this type of linear indication, and be rejected if it is found, even if no actual separations occur during solder float testing.

The "fine line" defect is characterized by the presence of a narrow faint line which extends across the full thickness of the foil. Defects associated with resin smear are not necessarily continuous, and often manifest themselves as dark spots or discontinuous lines at the barrel plating/innerplane junctions. Figure 36 illustrates four such defects affecting from virtually none to almost all of the junction, with the first one clearly acceptable, the last two clearly rejectable, and the second one perhaps open for debate. Just about every intermediate condition has been seen. It becomes a matter of judgement which coupons to accept and which to reject. For example, the junction shown in Figure 37 has a few isolated spots of contamination which are plainly seen in the unetched condition, but most of the junction is sound. In contrast, the junction illustrated in Figure 38 has a linear defect (in this case caused by epoxy smear) extending more than halfway across the junction. A small, rounded defect is considered less likely to propagate into an actual separation than is a linear flaw—much as minor porosity in a weld is not as severe a defect as is a crack. For non-linear defects, it comes down to a matter of whether the remaining cross-sectional area of the joint is sufficient to withstand the applied stress expected in service. The hole containing the junction shown in Figure 37 may be considered acceptable if that is the worst defect that it contains, while the hole shown in Figure 38 should be rejected.

One fact that supports a conservative interpretation of defects seen in board coupons is that an entire board, which may have several hundred holes, is being judged by scrutiny of less than 10 holes, even if all MIL-P-55110 examinations are performed. These holes are perforce assumed to be representative of the rest of the panel, and any defect noted in the sample holes must be assumed to exist in a statistically significant number of the holes on the panel, and may be present to a greater or lesser degree from one hole to the next.

PART III. NOTES ON METALLOGRAPHIC PREPARATION OF MULTILAYER BOARD TEST COUPONS

A suggested step-by-step procedure for preparing plated-through hole coupons for metallographic examination is included as Appendix B. An evaluation of a multilayer board is obviously valid only if the coupon is properly prepared and examined. The procedures involved, while simple, are not necessarily easy, and inexperienced personnel will have difficulty both in producing a good quality polished cross section and in recognizing when they have done so. Metallography is an art rather than a science, and while there is no substitute for experience, certain pitfalls can be avoided if the rationale behind certain of the steps is understood.

The first step is to cut the desired holes from the test coupon. Cuts made too far from the hole will entail a lot

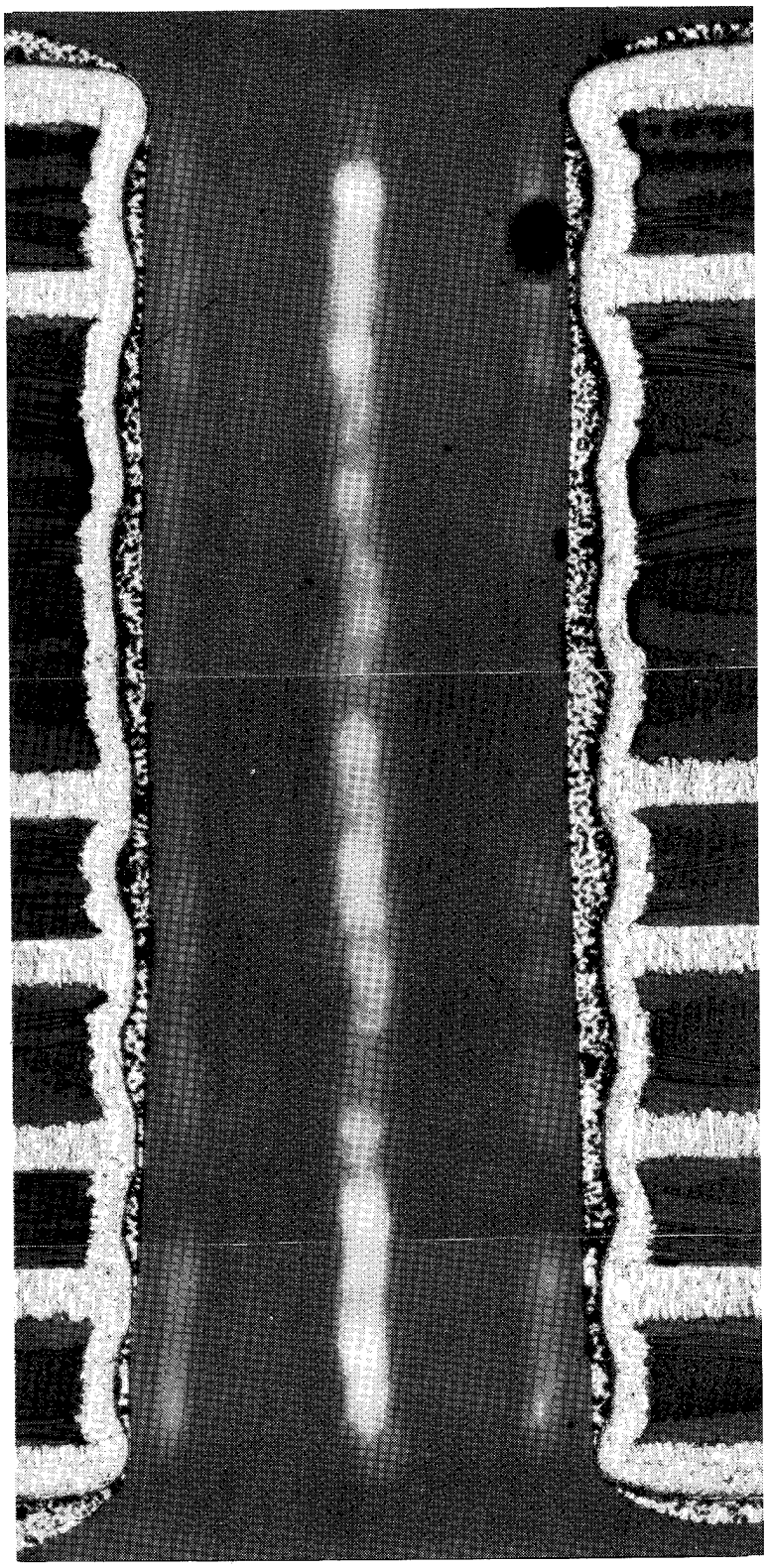


Figure 31. Overall view of plated-through hole at 100X, etched.

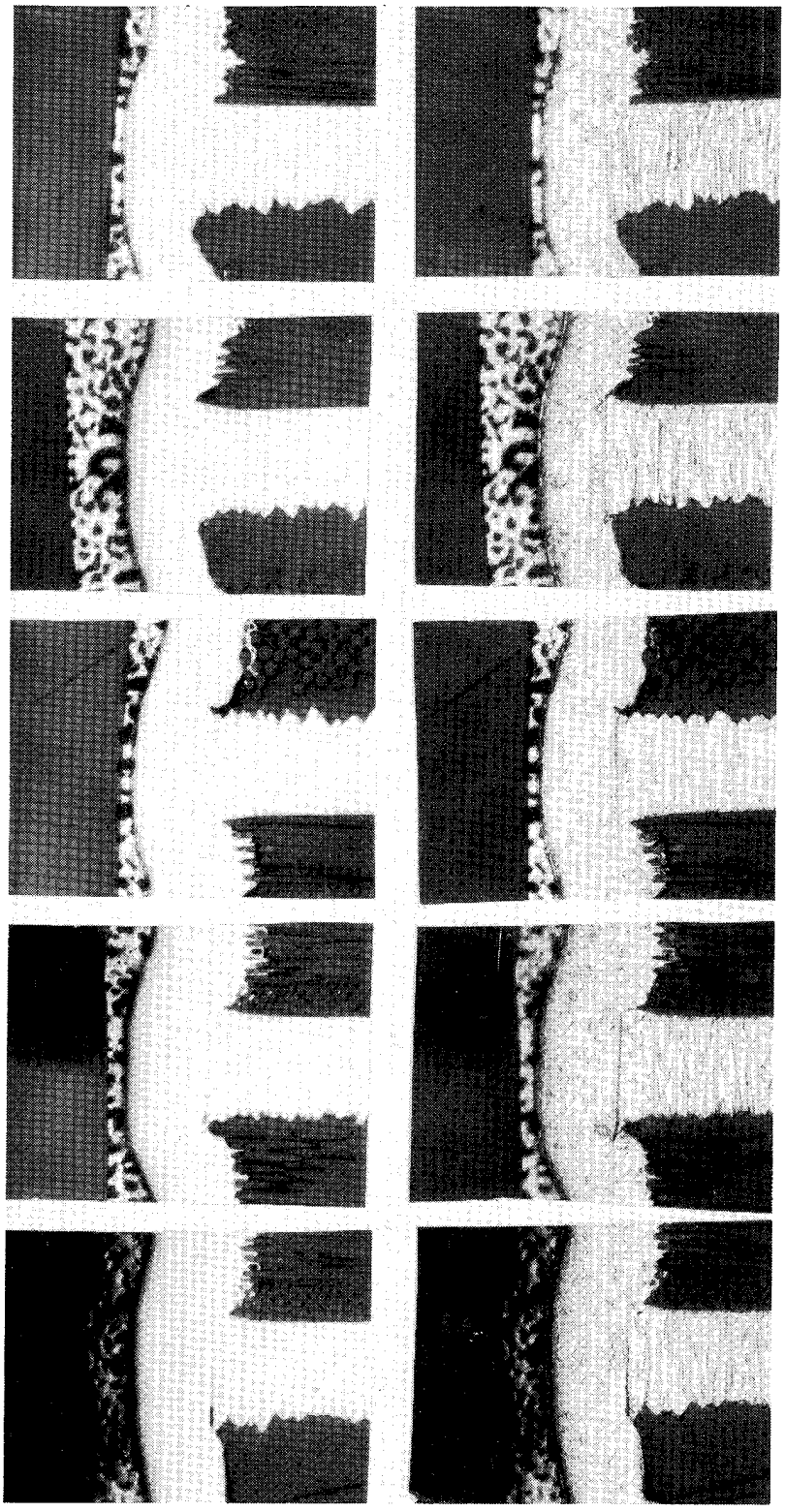


Figure 32. Barrel/innerplane junctions from the coupon illustrated in Figure 31 unetched (left) and etched (right), all at 200X.

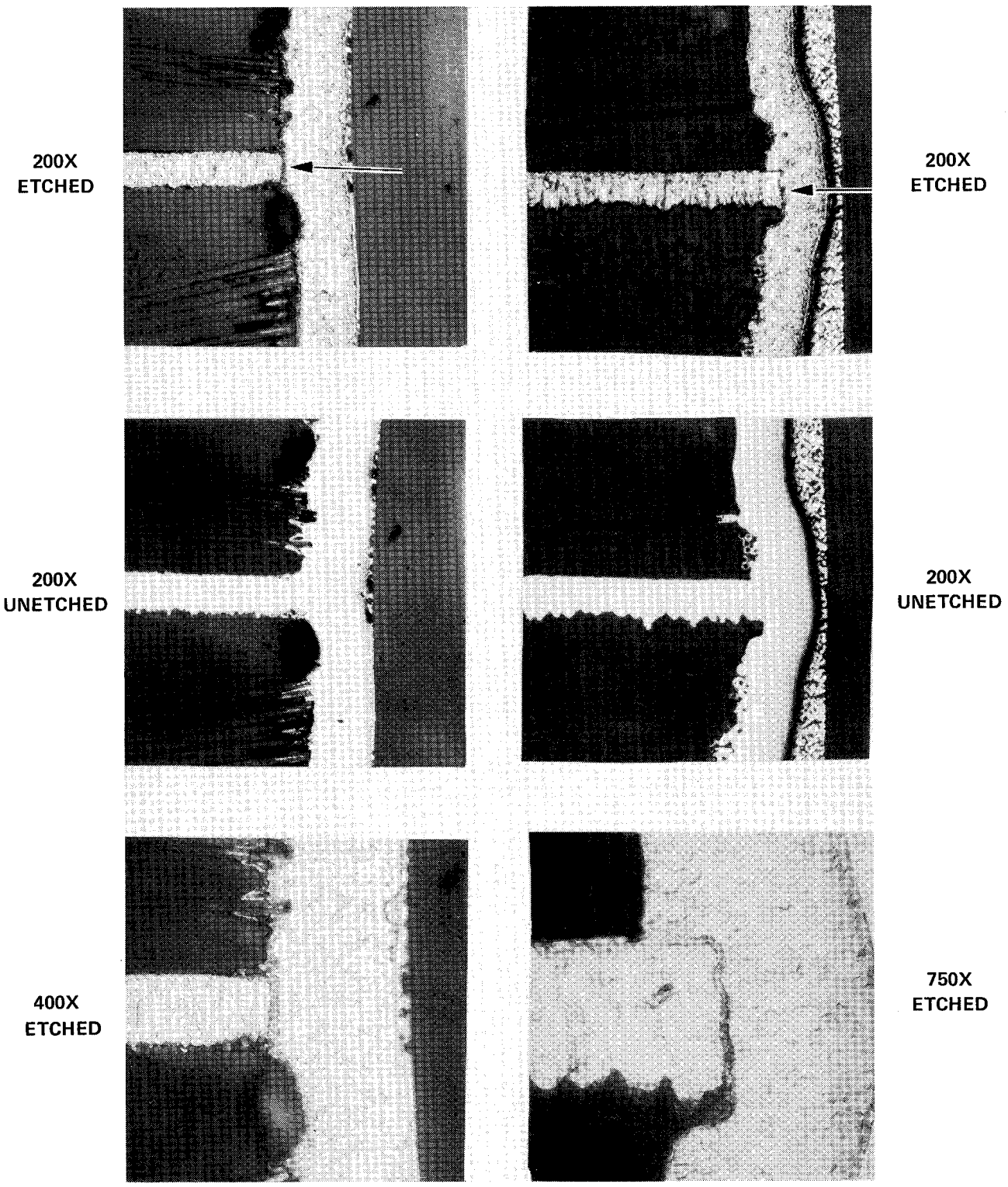


Figure 33. A dark-etching copper strike layer may be mistaken for a separation if the coupon is examined at low or moderate magnification after etching.

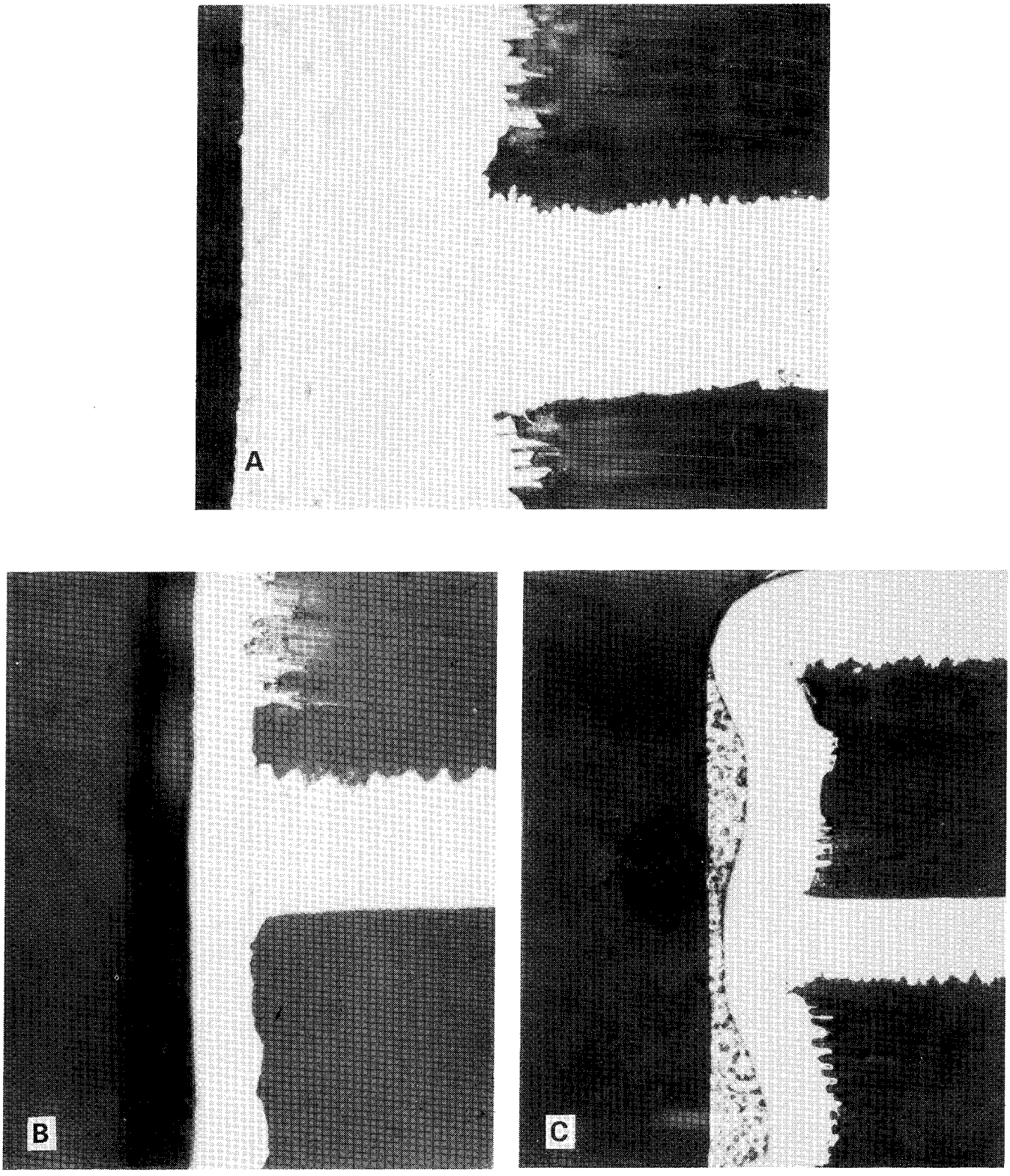


Figure 34. Visible demarcation lines at barrel/innerplane junctions ("fine line" defects) seen prior to etching. Coupons were not solder float tested. A – 500X; B – 400X; C – 200X.

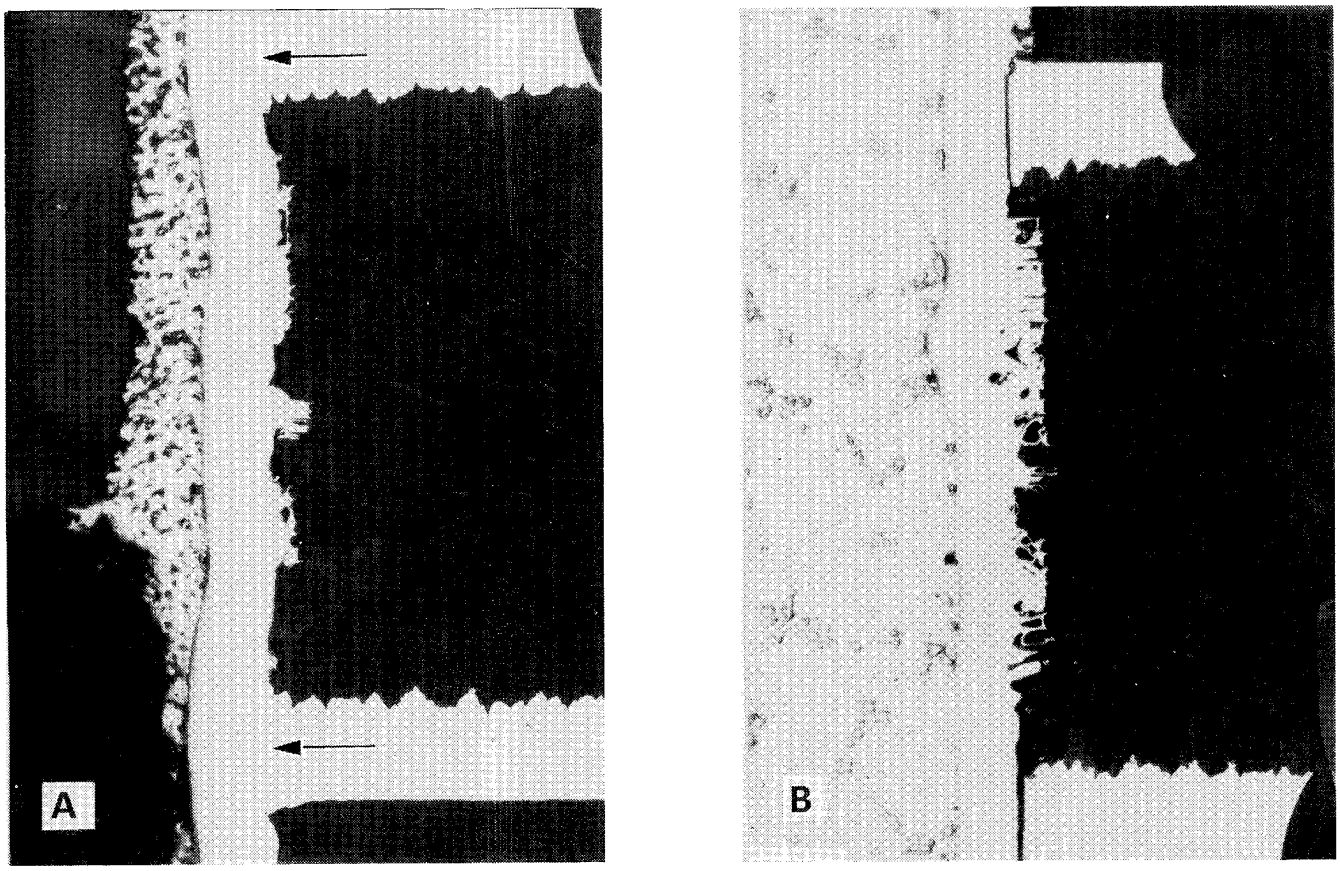


Figure 35. Coupons which exhibit fine line defects before solder float testing may show separations after thermal stress.

A. Continuous fine line defects before solder float. Unetched, 200X.

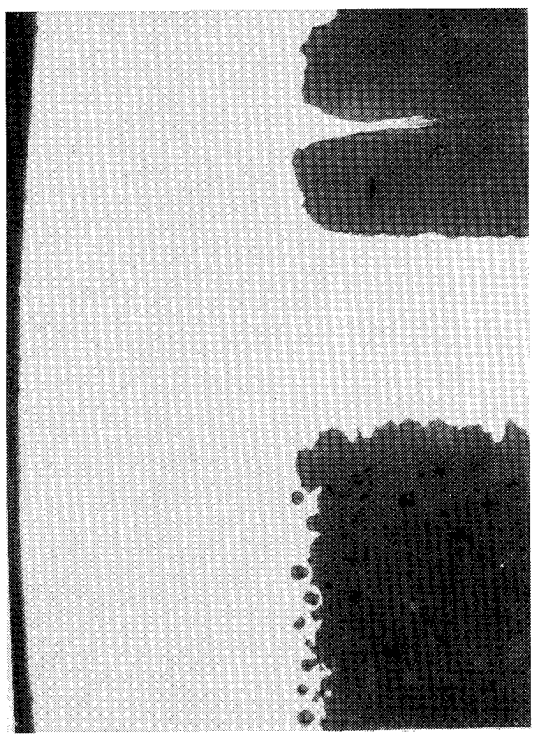
B. Another hole from same coupon after solder float. Weak bonds have opened up. Unetched, 200X.

of grinding after the specimen is encapsulated, leading to an increased probability of failure to maintain the axis of the hole parallel to the surface of the mount. Cuts made through the hole destroy it, and cuts made too close will induce damage in it. In particular, shearing close to a PTH will cause delamination. A good compromise is to make a gentle cut right at the edge of the terminal pad. One may use a low-speed (about 300 rpm) diamond wafering saw with cutting fluid, or one may hand cut, dry, using a jeweler's hacksaw with a fine blade. The finer the blade, the less chance of generating too much heat or causing mechanical damage to the hole—the blade breaks first! A hand-sawn surface may require smoothing on 240 grit wet-or-dry silicon carbide paper. All grinding and polishing steps should be done wet to avoid excessive heat buildup.

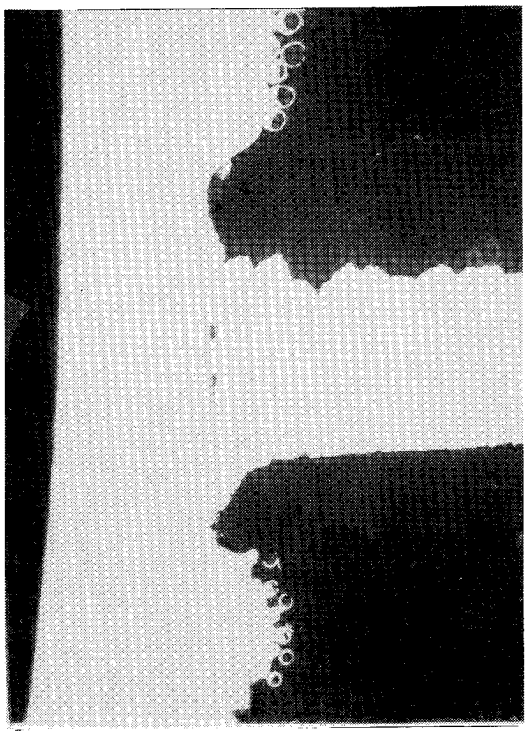
There are many methods of positioning the cut specimen so that it will maintain the correct alignment during the encapsulation process (mounting). Short sections of thick boards will stand unsupported; all manners of clips, springs and holders are commercially available or may be improvised. For example, tinned copper wire may be bent to a U-shape to hold one or more coupons upright in the mount. Plastic, copper and stainless steel are all acceptable for use as supports. Other metals should be avoided because they might interfere with the chemistry of the etching process.

It is essential that the mounting material chosen be a room temperature curing resin requiring no pressure. Elevated temperatures and pressures will alter the coupon to an unacceptable degree and render it worse than useless for evaluation purposes (worse because misleading information is worse than none). Some fast-setting epoxies have excessive exothermic reactions and should be avoided, but the choice of resin is not otherwise important, nor are the details of ring molds and such.

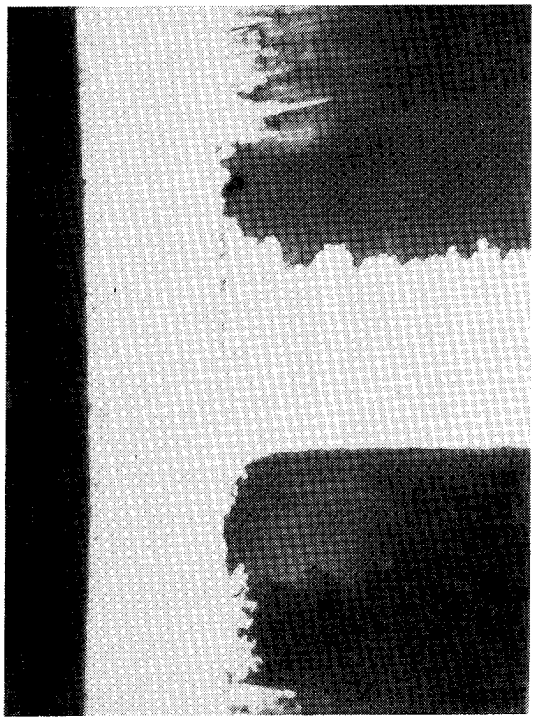
Keeping track of coupon identity is facilitated by scribing the serial number or other identification on the portion of the test coupon to be microsectioned before cutting it



GOOD: NO VISIBLE DEFECTS



MARGINAL (?) ~10% DEFECTIVE



MODERATELY SEVERE: 10 – 50% DEFECTIVE

SEVERE: > 50% DEFECTIVE

Figure 36. Examples of defect levels at barrel/innerplane junctions. All unetched, at 400X.

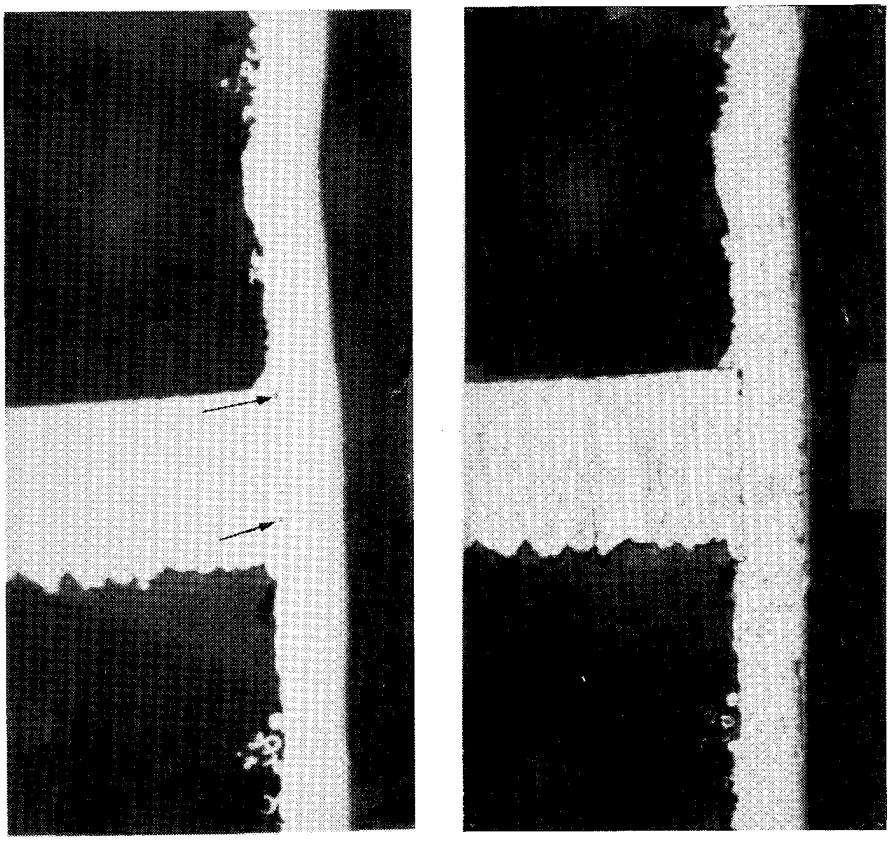


Figure 37. Minor point defects at barrel/innerplane junction visible in unetched condition would probably not be noticed in etched condition. These isolated small spots are not so worrisome as linear defects, and this hole could be accepted if other criteria are met. Left – unetched, 200X. Right – etched, 200X.

off from the rest of the coupon. After mounting, the necessary information together with the metallographer's initials and the date should be promptly scribed on the back of the mount. If more than one coupon is to be put in the same mount it is sometimes convenient to arrange them by serial number, and trim the lowest numbered pieces slightly shorter than the next, and so forth, so that there is no identity crisis when observing the polished face of the mount, even though the numbers are scribed on the other side.

It is easier to maintain flatness while grinding and polishing if the specimen is broader than it is tall–for a 1¼ inch diameter mount, a convenient height is about ¾ inch–too short is hard on the fingertips. It is helpful to round the edges of both the top and the bottom of the mount: the top for operator comfort and the bottom to minimize snagging on the polishing cloths.

The grinding steps are very important and should not be slighted. A belt grinder with a 240 grit belt may be used for rapid material removal down to where the pads become visible. Care must be taken to provide sufficient coolant to prevent overheating the epoxy both of the mount and the board laminate. At this point is is safer to switch to hand grinding to avoid inadvertently grinding too far. Grinding pressure should lessen as the grit size becomes finer. All grinding steps, however carefully done, produce some subsurface damage which must be removed by the succeeding steps. This is the reason for specifying that the specimen be ground on each grit for twice the length of time it takes for the prior grit scratches to be removed.

The polishing steps will be relatively short on a properly ground specimen, on the order of a few minutes. It is convenient to have a three-station polishing table, and to use, for example, the right hand wheel for 1 micron alumina, the middle one for 0.3 micron, and the left one for 0.05 micron. A dispensing bottle containing a slurry of the appropiate micron size should be kept near the wheel used for that grade, in a position where it is difficult or awkward to reach from either of the other two wheels. These precautions are especially valuable if more than one person uses the polishing area. Liquid hand soap or dishwashing liquid, diluted with water, may be used as a lubricant on the final two wheels to minimize smearing and to facilitate polishing. The details of how wet or dry the polishing cloth should be, what pressure to use, and how long to pol-

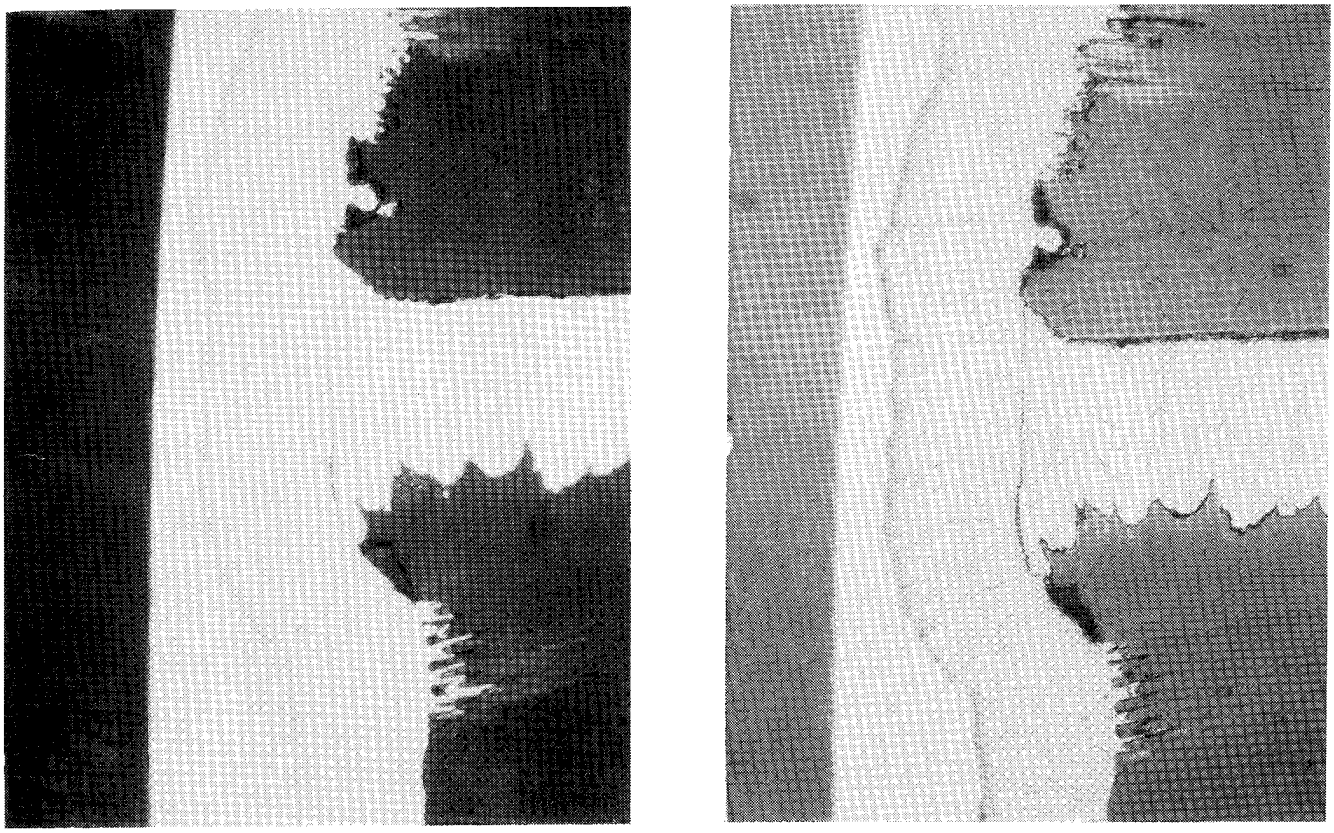


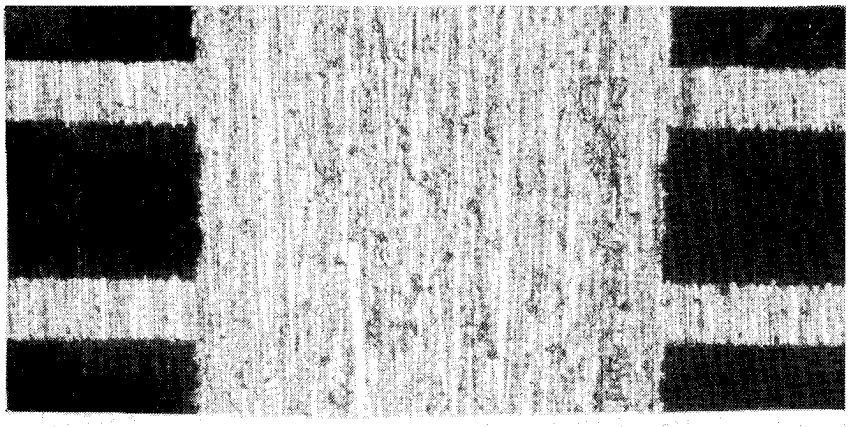
Figure 38. Linear defect extending more than halfway across junction is at least partly masked by etching. Note also the undesirable columnar plating microstructure. This hole should be rejected. Left – unetched, 400X; Right – etched, 400X.

ish can only be worked out by experience. Specimens should be checked at 50 – 100X after each polishing step to ensure that the effects of the prior step have been completely removed. Figure 39 illustrates the typical appearance of specimens after 600 grit, 1.0, 0.3 and 0.05 micron alumina steps.

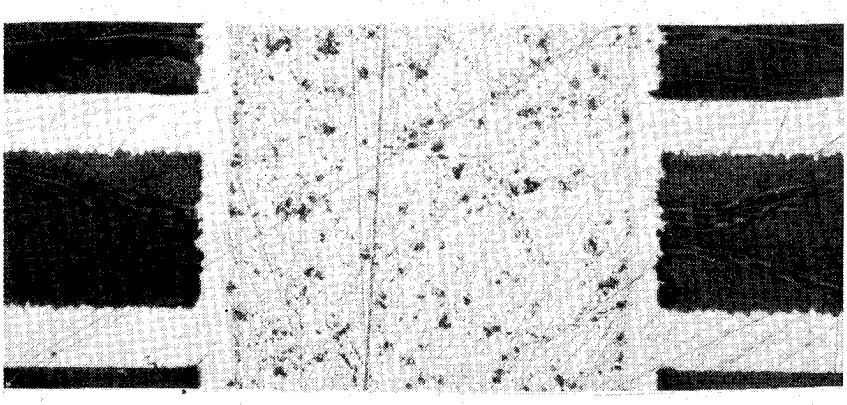
Much time can be wasted and poor results achieved if too much time is spent on the final wheel trying to compensate for lack of adequate intermediate grinding and polishing steps. The coupon shown in Figure 40 does not have laminate voids: the pits in the laminate represent the deepest parts of coarse grit scratches which were not fully removed in the subsequent steps. Polishing time should be kept as short as possible to minimize the inevitable edge rounding, especially of the hole plating, which results from the different polishing rates of the laminate, copper, solder, and mounting material. Laminate voids are exaggerated by edge rounding caused by overpolishing, and plating thickness can become difficult to measure accurately. If there is doubt as to whether an observed feature is real or is an artifact of preparation, the safest course is to regrind on 600 grit paper and repolish.

One other area of concern is the solder float testing of the coupon. The procedure given in Paragraph 4.8.6 is quite plain in that it details what the time and temperature exposure of the coupon should be. The conditioning bakeout is designed to remove moisture from the laminate so that spurious measling, blistering, and laminate voids caused by vaporizing of adsorbed water will not occur. The bakeout time has been extended from 2 hours to 6 in Revision D of MIL-P-55110. Times in excess of 6 hours should not be used, since some degradation of the laminate may occur with prolonged exposure to the bakeout temperature. It is easier to conduct this test if the following hints are observed. First, cut the coupon so that ample space is provided around the holes. If the cut is too close to the hole, excessive damage may occur. Then, insert a convenient length of wire into one of the holes so as to form a handle, bent at 90 degrees to the plane of the board, to be used to place the coupon on the molten solder, and to pick it up again. At the conclusion of the test, this hole will have a wire soldered into it, and therefore does not represent a standard test configuration. In the usual course of events, two rows of holes will be present in the coupon, and this

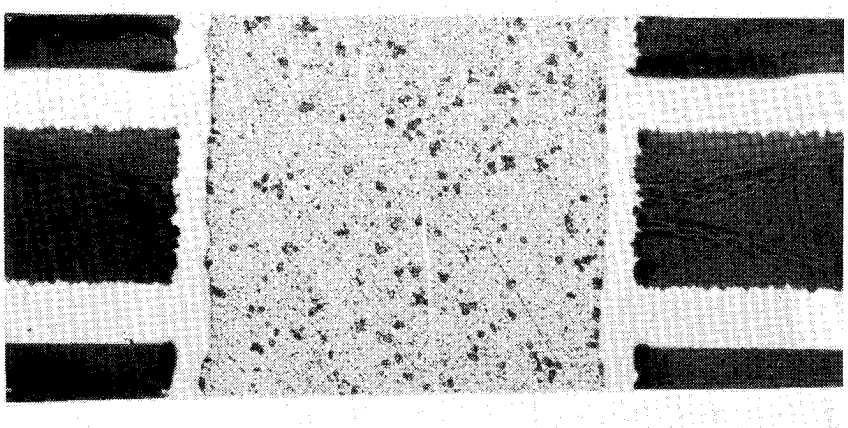
600 GRIT FINISH



1 MICRON ALUMINA FINISH



0.3 MICRON ALUMINA FINISH



0.05 MICRON ALUMINA FINISH

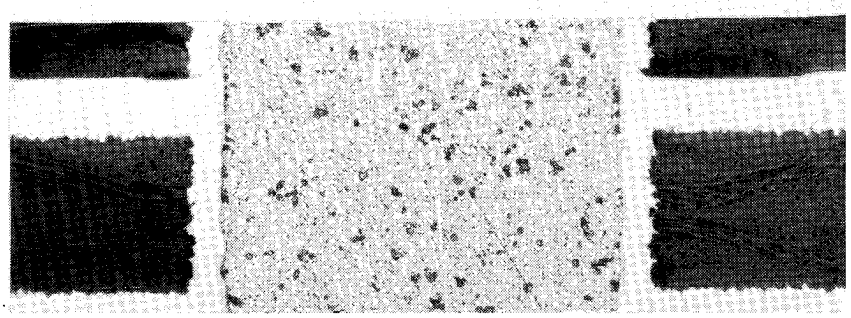


Figure 39. Typical appearance of specimen at various stages of preparation. All at 75X.

wire can be oriented in the specimen mount as the second (or backup if disaster strikes the sectioning procedure) row of holes. This hole may be disregarded in the evaluation, but it can provide a good clue as to what will happen when in service a component lead is soldered into the hole. Liquid flux is conveniently applied to the coupon with a cotton swab. It is handy to keep a piece of circuit board, about 1 – 2 inches square, to sweep the slag off the surface of the molten solder immediately before floating the coupon. A correctly fluxed and floated coupon will have the holes completely filled with solder after this test. After cooling to room temperature, the coupon is trimmed to expose the edges of the terminal pads and processed in the same manner as the as-received specimens.

A 1:1 mixture of 3% hydrogen peroxide and concentrated ammonium hydroxide is satisfactory for use in etching multilayer board coupons. The chemicals must be fresh, and freshly mixed. One procedure is to keep small quantities of peroxide and ammonia in dropper bottles and to mix 10 drops of each in one of the depressions in a ceramic spot plate. The etchant is applied by gently swabbing for approximately five seconds. A vigorous bubbling should occur. Rinse well in hot tap water and blow dry. Discard the solution and mix fresh if more than five to ten minutes elapse between usages. The presence of an orange stain on the specimen indicates that the chemicals are no longer fresh.

When examining plated-through hole coupons and photographing the microsections, it is frequently helpful to deposit a thin gold, or other metal, coating on the specimen to enhance the reflectivity of the laminate with respect to the metallic portions of the specimen. A sputtered coating such as is given to scanning electron microscope specimens is appropriate. This is especially valuable when illustrating laminate voids at the same time as plating quality. Figure 41 compares uncoated and gold-sputtered specimens. Caution: make sure the specimen is thoroughly dry before exposing it to the vacuum of the sputtering apparatus; otherwise, residual liquids will spread over the surface.

When the specimen has been adequately polished, but not etched, the microsection evaluations described in Part II can begin.

PART IV. OUTLINE OF SUGGESTED PROCEDURE

1. Include as-received and solder float tested specimens from each coupon in one mount. Use techniques of Appendix B.
2. Polish and examine, before etching, at 100X for:
   a. Layer to layer registration
   b. Laminate voids and delaminations (use appropriate criteria for as-received and solder floated specimens)
   c. Resin recession
   d. External annular ring
   e. Nodules and glass fiber protrusion
   f. Dielectric layer thickness and thermal plane spacing
   g. Measles and lifted lands
3. Increase magnification to 200X and check for:
   a. Plating thickness
   b. Barrel/innerplane junction integrity: resin smear, separations, fine line defects
   c. Cracks in conductive surfaces
   d. Plating voids
4. If in doubt, especially as regards barrel/innerplane defects, increase magnification to 400X
5. Etch specimen and examine at 100-200X for:
   a. Hole plating microstructure
   b. Cracks in conductive surfaces
   c. Etchback
   d. Internal annular ring
6. If it is necessary to repolish after etching, regrind on 600 grit so as to remove all etching effects, especially at the barrel/innerplane junctions, which tend to etch deeply.

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2. Einarson, Norman S., *Printed Circuit Technology*, Prnted Circuit Technology, Burlington, MA, 1977.
3. Smith, George, "The Thermal Zone Concept," PC FAB, December 1983.
4. Kirschenbaum, Jerry and Fairbanks, Cathy, "The Effect of Amendment 5 on MIL-P-55110D," IPC-Technical Review, March, 1984.

ACKNOWLEDGMENT

The unflagging support and expert metallographic assistance of Ms. Diane M. Kolos of the Materials Branch, GSFC, is gratefully acknowledged.

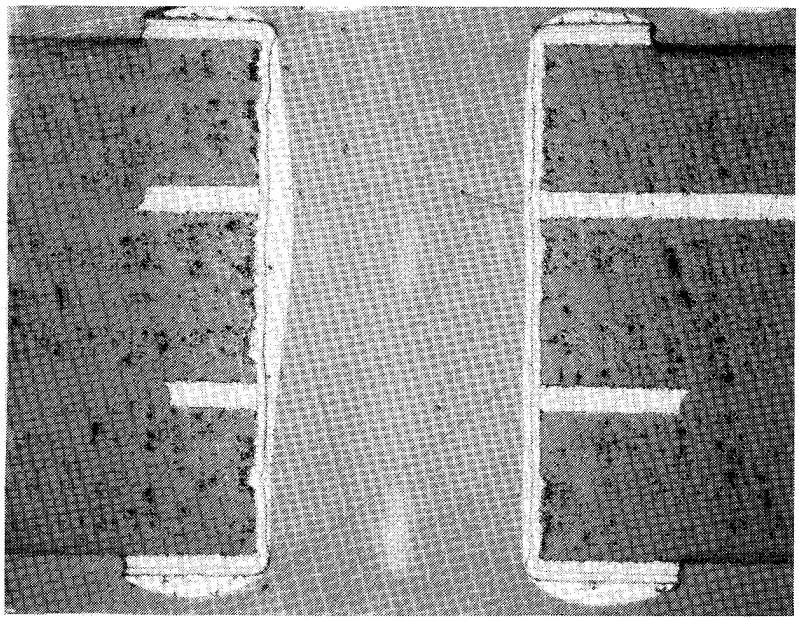


Figure 40. Incomplete removal of coarse grit grinding scratches leaves artifacts which may be mistaken for laminate voids. Etched, 50X.

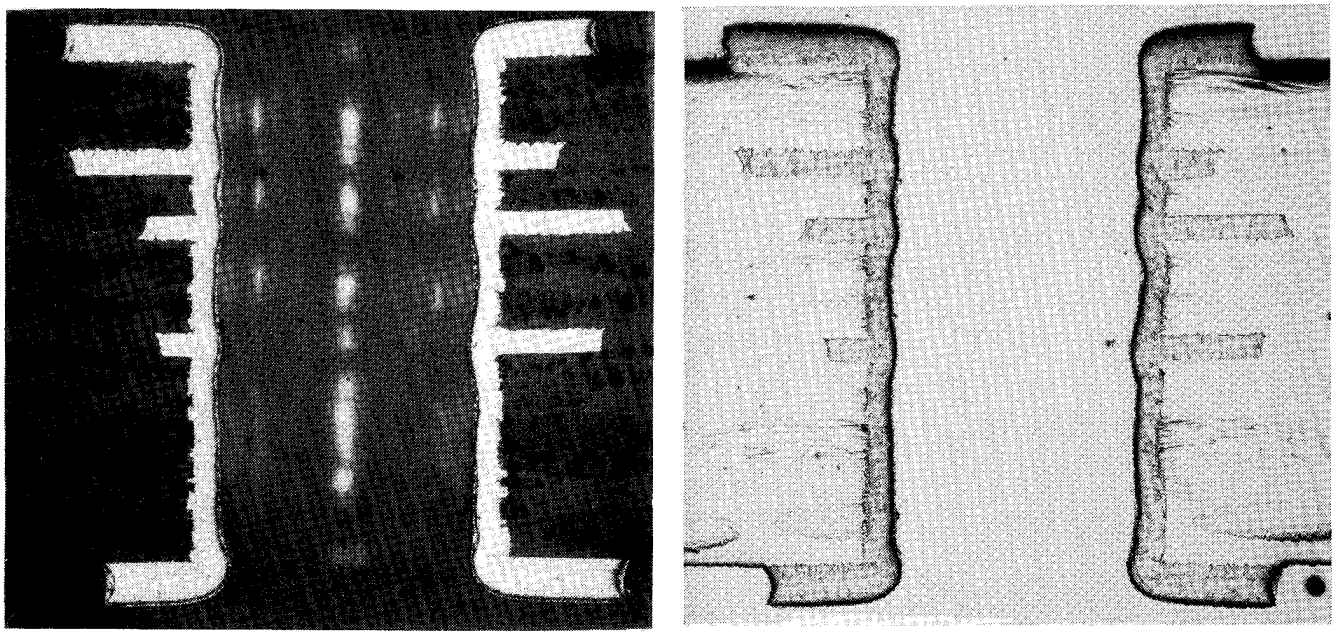


Figure 41. A sputtered gold coating enhances reflectivity of the laminate. Uncoated (left) and coated (right) at 50X.

INDEX

APPENDIX A

SECTIONS OF MIL-P-55110D PERTAINING TO CROSS-SECTIONING PLATED-THROUGH HOLES

* * * DEFINITIONS * * *

6.7 Definitions

6.7.1 Terms and definitions: The definitions of all terms used herein shall be specified as IPC-T-50 and the following:

6.7.1.1 Bulge: A bulge is a swelling of a board usually caused by internal delamination or separation of fibers.

6.7.1.2 Circuitry layer: A circuitry layer is a layer of a printed board containing conductors. It also includes both ground planes and voltage planes.

6.7.1.3 Composite board: a composite board is a completely laminated multilayer printed board.

6.7.1.4 Contract service(s): Contract services are those services contracted or performed (or both) outside the qualified manufacturer's immediate facility, not to include laboratory and electrical function tests.

6.7.1.5 External layer: An external layer is a conductor pattern or land on the surface of the composite board.

6.7.1.6 Nick: A nick is a small cut in the edge of a conductor.

6.7.1.7 Nodule: A nodule is a rounded mass of irregular shape; a little lump.

6.7.1.8 Nominal cured thickness: The nominal cured thickness is the thickness of a laminate or multilayer board after the prepreg has been cured at the temperature and pressure specified for that particular class of resin flow.

6.7.1.9 Pregelation particles: Pregelation particles, white spots which do not propagate as a result of any soldering operation, are acceptable regardless of location.

6.7.1.10 Plating lot: A plating lot is defined as any number of boards or composite panels that are placed in any one plating tank and are processed through that one particular plating cycle.

6.7.1.11 Resin starvation: Resin starvation is a deficiency of resin in base material that is apparent after lamination by the presence of weave texture.

6.7.1.12 Sequential lamination: A type of multilayer printed-circuit board, consisting of several individual single- or double-sided boards laminated together. Each double sided increment usually contains via holes; and the entire laminated assembly usually contains plated-through holes which are through connections. "Sequential lamination" is a final assembly, with plated-through holes, composed of individual multilayer or double-sided boards which may contain plated-through holes.

6.7.1.13 Sequential laminating process: A process for making multilayer printed-circuit boards by laminating increments of double-sided boards together. [For details, refer to MIL-P-55110D].

6.7.1.14 Sequential plating process: A process for manufacturing multilayer printed-circuit boards, in which alternate layers of metallic circuitry and dielectric insulating material are built up by processes such as electroplating, screen printing, laminating, etc., with conductor layers interconnected as may be required. [Balance of definition discusses distinctions among various terms describing multilayer board fabrication processes.]

6.7.1.15 Sliver: A sliver is a slender metallic projection that has been separated from the edge of a printed-circuit conductor.

6.7.1.16 Splay: Splay is the tendency of a rotating drill bit to drill off-center, out-of-round, non-perpendicular holes.

6.7.1.17 Touching up: Touching up is the act of manually repeating a manufacturing operation for the purpose of improving the yield of acceptable parts.

6.7.1.18 Wrinkle: A wrinkle is a crease or fold in one or more outer layers of a laminated plastic (copper foil, fabric, paper, conformal coating, etc.) that has been pressed in.

* * * QUALITY CONFORMANCE INSPECTION * * *

4.7 Quality conformance inspection: Quality conformance inspection shall consist of inspections on the production boards and the quality conformance test coupon area in tables VII and IX for groups A and B inspections. Selection of test coupons for testing shall be in accordance with tables VII and IX. Each production board or panel of boards shall incorporate the quality conformance test coupons as specified on the master drawing. Unless otherwise specified, quality conformance test coupons used in performing group B inspection shall be retained by the manufacturer. Unless otherwise specified, test patterns used in performing group A inspection and all unused quality conformance test coupons shall be retained for 3 years.

4.7.1.2 Group A inspection: Group A inspection shall consist of the inspections specified in table VII. For type 3 [multilayer boards], 100 percent inspection per panel shall be performed for thermal stress. See table VII for sampling levels for type 1 and 2 boards.

4.7.1.3 Group B inspection: Group B inspection shall consist of the inspections specified in table IX at a laboratory which has obtained laboratory suitability status from the cognizant qualifying activity (DESC-EQ). Group B inspection shall be made on sample units selected randomly from inspection lots which have passed group A inspection.

* * * DETAILS OF REQUIREMENTS AND PROCEDURES * * *

3.6.6 Layer-to-layer registration (see figure 1). Unless otherwise specified on the master drawing, layer-to-layer pattern misregistration, shall not exceed 0.014 inch (0.36mm) when measured in accordance with 4.8.3.5 using one of the methods of 4.8.3.5.1 through 4.8.3.5.3.

4.8.3.5 Layer-to-layer registration (see 3.6.6). Layer-to-layer registration shall be determined by microsectioning of coupons, or by test of special registration coupons when provided, or by visual assessment involving observations and comparative measurements of land relationships visible at or just below the board surface.

4.8.3.5.1 Microsectioning. Two coupons from diagonally opposing panel corners shall be evaluated in accordance with 4.8.1.2. Registration shall be measured at a magnification of 100X ± 5 percent after microsectioning both coupons in the vertical plane, but one coupon is to be sectioned in the panel's length direction while the other is to be sectioned in the width direction. These microsections shall be evaluated by computing the difference in centerline location of the two lands found to be most eccentric to one another within each section (see figure 1).

4.8.1.2 Microsection inspection: Microsection inspections (such as plated-through hole, plating thickness, and foil thickness) shall be accomplished using methods in accordance with either IPC-TM-650, method 2.1.1 or ASTM B-487. Automatic microsectioning techniques may be used in lieu of IPC-TM-650 or ASTM B-487 (see 4.8.1.2.1).

4.8.1.2.1 Microsectioning and inspecting. Plated-through holes shall be microsectioned in the vertical plane at the center of the hole ± 10 percent and inspected for foil and plating integrity at a magnification of 100X. Referee inspections shall be accomplished at a magnification of 200X. Each side of the hole shall be viewed independently. A minimum of one microsection containing at least three holes shall be made for each sample tested. Inspection (such as laminate thickness, foil thickness, plating thickness, solder coating, lay-up orientation, laminating, resin smear and plating voids) shall be accomplished at magnifications specified above. If resin smear is detected or suspected on a vertical microsection, a referee microsection shall be prepared and evaluated in the annular (horizontal) plane.

4.8.1.2.2 Measurements. Measurements shall be reported as the average of three determinations per each side of the hole. Isolated thick or thin sections shall not be used for averaging; however isolated areas of reduced copper thickness shall be measured and shall meet the requirements of 3.8.2 and 3.8.3. [p. A-3 of this document]

3.6.6.1 Special registration test coupons. Special registration test coupons may have been designed into the board or panel by the design activity, or may be added to the panel to enhance testability. Refer to 4.8.3.5.2. See MIL-STD-275 for examples. To be usable for acceptance purposes, special registration coupons must relate the actual grid location of each circuitry layer to all other layers and to the hole pattern accuracy attained (see 3.6.2) in each board. [3.6.2 says hole pattern accuracy shall be as on master drawing.]

4.8.3.5.2 Special registration coupons (see 3.6.6.1). If special registration coupons and requirements are provided as an element of the design documentation set, registration shall be evaluated in accordance with the criteria specified on the master drawing. Special registration coupons, when provided by the board fabricator, shall be evaluated in accordance with methods approved by the acquiring activity. Unapproved methods of measurement using applied coupons shall be backed up by the method of 4.8.3.5.1 [microsectioning; see above] using appropriate coupons from the same panel.

3.6.6.2 Visual Assessments. For type 2 boards, and certain type 3 boards having 6 or fewer layers, registration can be inspected in accordance with 4.8.3.5.3 and verified to meet requirements of 3.6.6 uisng the method of 4.8.3.5.3.

4.8.3.5.3 Visual assessment of registration (see 3.6.2). Layer-to-layer registration of type 2 boards shall be satisfied if both the outer layers pass the external annular ring inspection of 4.8.3.6 [see below] and if the hole pattern accuracy inspection of 4.8.3.1 [references 4.8.1, visual inspection of board at low magnification] is also acceptable. Type 3 boards with 4.8.3.6 and 4.8.3.1 conforming on the outer layers may be viewed under a combination of bottom (transmitted) and overhead lighting. Each internal layer must be observable from one or the other side of the board and must be visually comparable, land to land, to the surface pattern at two through-hole locations, minimum. These two locations must span at least 80 percent of the diagonal length of the land pattern on a board or panel (or both). If the internal layer lands at these locations can be seen to readily meet the annular ring criteria of 3.8.7 [0.002 inch minimum, see figure 2] using visual comparison to the surface land condition, the board's registration is also acceptable to 3.6.6. Referee measurements shall be made in accordance with 4.8.3.5.1 [microsectioning] in the event of any uncertainty in making the visual comparisons at up to 10X magnification.

3.6.7 Annular ring (external). When evaluated in accordance with 4.8.3.6, the minimum external annular ring may have in isolated areas a 20 percent reduction of the minimum annular ring specified in 3.6.7.1 and 3.6.7.2, due to defects such as pits, dents, nicks, pinholes.

3.6.7.1 Annular ring (unsupported hole) (see figure 2). The minimum annular ring for an unsupported hole shall be 0.015 inch (0.38mm).

3.6.7.2 Annular ring (plated-through hole) (see figure 2). The minimum annular ring for a plated-through hole in type 2 and external layers of type 3 boards shall be 0.002 inch (0.05mm), except adjoining to the conductor run where there will be 0.005 inch (0.13mm) minimum annular ring.

4.8.3.6 Annular ring (external) (unsupported and plated-through holes) (see 3.6.7). When inspected in accordance with 4.8.1 [visual examination performed on board at 4X], the measurement of the annular ring on external layers is from the inside surface (within the hole) of the plated hole or unsupported hole to the outer edge of the annular ring on the surface of the board.

3.6.9 Plating and coating thickness (see 4.8.3.8). Unless otherwise specified on the master drawing, plating or coating thickness shall be in accordance with table I and inspected in accordance with 4.8.1 and 4.8.1.2 or 4.8.3.8. After tin-lead is fused or solder is reflowed, no measurement of plating thickness is required, but solderability in accordance with IPC-S-804 (see 4.8.2.6.1, 4.8.2.6.2 [references IPC-S-804]) shall be performed and visual inspection of complete copper coverage shall be performed. Complete copper coverage by solder does not apply to the vertical conductor edges.

4.8.3.8 Tin-lead plating or solder coating thickness (see 3.6.9.). Solder coating or tin-lead plating, prior to fusing or reflow, thickness shall be measured at least four times, one in each quadrant of a panel or each quadrant of a plated-through hole microsection.

3.8 Construction integrity (by microsection evaluation of as-received production boards, coupons, and qualification specimens prior to stress) (see 4.8.5). The three plated-through holes shall be inspected in the vertical cross-section in accordance with 4.8.5. Figures 3 through 9 show the plated-through hole structure evaluation.

4.8.5 Construction integrity (through microsection inspection prior to stress) (see 3.8).

3.8.1 Plated-through hole (see 4.8.5.1 and figure 3). When inspected in accordance with 4.8.5.1, finished boards, supporting coupons, and qualification test specimens shall meet the requirements of 3.8.1 through 3.8.11. After having been subjected to thermal test stresses as specified in 3.9.1, the additional criteria of 3.9.1 apply. Board testing is destructive and reserved to referee situations. In general, good workmanship and technique should be evident; the following requirements apply in this respect:

a. There shall be no cracks in the conductive foils, platings, or coatings.
b. There shall be no separations at conductive interfaces.
c. Nail-heading shall not exceed one and one-half times the foil's thickness.
d. Nodules, plating folds, or plated glass fiber protrusions that project into the hole shall be acceptable provided that the hole diameter and the copper thickness are not reduced below their respective limits.

4.8.5.1 Plated-through hole inspection (see 3.8.1). After meeting the requirements of 3.5.4 [marking] and 3.5.5 [workmanship] and inspected in accordance with 4.8.1.2 [p. A-2], the holes shall be microsectioned and inspected and meet the requirements of 3.8.1 (see figure 3).

3.8.1.1 Thermal planes. When inspected in accordance with 4.8.5.1.1, the minimum lateral spacing between adjacent conductive surfaces (non-functional lands) or plated-through hole and thermal plane shall be 0.004 inch (0.09mm) minimum.

4.8.5.1.1 Thermal planes. The lateral dielectric spacing between the heat sinking planes and adjacent conducting surfaces (non-functional lands) or plated-through holes shall be measured at the closest point between these surfaces or the plated-through hole and shall meet the requirements of 3.8.1.1 when inspected in accordance with 4.8.1.2 [microsection].

3.8.2 Plated copper thickness. Unless otherwise specified on the master drawing, plated deposits shall be in accordance with table III and inspected in accordance with 4.8.5.2 (see figure 4).

4.8.5.2 Plating thickness (see 3.8.2). Plating thickness on the surface and in the plated-through hole shall be inspected in accordance with 4.8.5.1. Plating measurements in the plated-through hole shall be reported as the average of three determinations per each side of the hole. Isolated thick or thin sections shall not be used for averaging. However, isolated areas of reduced copper thickness shall be measured and meet the requirements of 3.8.2 (see figure 4).

3.8.3 Plating voids. When inspected in accordance with 4.8.5.3, the plating in the plated-through hole shall not exhibit any voids. If voids are present in the microsection, the lot shall be 100 percent visually inspected in accordance with 4.8.1. Following 100 percent visual inspection, any board with a hole having more than three plating voids shall be rejected. In addition, the combined length of the voids shall not exceed five percent of the total wall length and the combined area of the

voids shall not exceed 10 percent of the total barrel surface area (see figure 5). Any board with a hole having a circumferential void shall be rejected.

4.8.5.3 Plating voids (see 3.8.3). Plating voids shall be inspected in accordance with 4.8.5.1 (see figure 5).

4.8.1 Visual and dimensional inspection. [visual examination of boards at low magnification]

3.8.4 Conductor thickness. The conductor thickness on printed wiring shall be as specified on the master drawing and inspected in accordance with 4.8.5.4.

4.8.5.4 Conductor thickness (see 3.8.4). Conductor thickness shall be inspected in accordance with 4.8.5.1.

3.8.5 Etchback or smear removal (type 3). When tested as specified in 4.8.5.5, plated-through hole shall be free of resin smear.

3.8.5.1 Hole cleaning (smear removal). When etchback is not specified on the master drawing, the hole shall be cleaned to meet the requirements of 3.8.5. Lateral removal of material from the hole wall shall not exceed 0.001 inch (0.03mm).

3.8.5.2 Negative etchback. A negative etchback of 0.0005 inch (0.013mm) shall be allowed provided the specimen meets the requirements of 3.9.1 following the thermal stress test (see figure 6).

3.8.5.3 Etchback. Only when specified on the master drawing, boards shall be etched back for the lateral removal of resin and glass fibers from the internal conductors prior to plating. When tested as specified in 4.8.5.5, etchback shall be 0.0002 inch (0.005mm) minimum and 0.003 inch (0.08mm) maximum when measured at the internal copper contact area protrusion with a preferred depth of 0.0005 inch (0.013mm) (see figure 6). Wicking may extend an additional 0.003 inch (0.08mm) provided it does not reduce the conductor spacing below the minimum requirements on the master drawing. The etchback shall be effective on at least the top or bottom surface of each internal conductor. Shadowing is permitted on external conductor only (see figure 6).

4.8.5.5 Etchback or smear removal (see 3.8.5). Etchback or smear removal shall be inspected in accordance with 4.8.5.1 (see figure 6).

3.8.6 Undercutting. When inspected in accordance with 4.8.5.6, undercutting at each edge of the conductors shall not exceed the total thickness of clad and plated copper, or 10 percent of the conductor width, whichever is smaller.

4.8.5.6 Undercutting (see 3.8.6). Undercutting shall be inspected in accordance with 4.8.5.1.

3.8.7 Annular ring (internal). When inspected in accordance with 4.8.5.7, the minimum annular ring for functional internal lands on type 3 boards shall be 0.002 inch (0.05mm).

4.8.5.7 Annular ring (internal) (see 3.8.7). The internal annular ring shall be inspected in accordance with 4.8.5.1 and measured as shown on figure 1. This measurement shall apply to all internal lands, both sides of the hole, for all three holes.

3.8.8 Dielectric layer thickness. The minimum dielectric thickness for types 1, 2, and 3 printed-wiring boards shall be as defined on the master drawing. Finished type 3 boards shall have a minimum of 0.0035 inch (0.089mm) of dielectric material between consecutive conductor layers (closest point between conductor layers), when cured (see figure 7). The dielectric material may be comprised of laminate, prepreg and laminate, or multiple layers of prepreg. Unless otherwise specified on the master drawing, there shall be no less than two sheets of prepreg (B-stage) or laminate (C-stage), or combination thereof, used between each pair of adjacent conductor layers. Dielectric layer thickness shall be inspected in accordance with 4.8.5.8.

4.8.5.8. Dielectric layer thickness (see 3.8.8). Dielectric layer thickness shall be inspected in accordance with 4.8.5.1. All measurements shall be made at the maximum point of dielectric thickness, which is typical of mechanical thickness measurements of base material (see figure 7).

3.8.9 Laminate voids. When inspected in accordance with 4.8.1.2 [p. A-2] and 4.8.5.9, finished printed-wiring boards shall have no delaminations in excess of that allowed in 3.5.3. Laminate voids with the longest dimension of 0.003 inch (0.08mm) or less shall be permitted.

4.8.5.9. Laminate voids (see 3.8.9). Laminate voids shall be inspected in accordance with 4.8.5.1.

3.8.10 Resin recession. When inspected in accordance with 4.8.5.10, resin recession at the outer surface of the plated-through hole barrel shall be permitted provided the maximum depth as measured from the barrel wall does not exceed 0.003 inch (0.08mm) and the resin recession on any side of the plated-through hole does not exceed 40 percent of the cumulative base material thickness (sum of the dielectric layer thickness being evaluated) on the side of the plated-through hole being evaluated (see figure 8).

4.8.5.10. Resin recession (see 3.8.10). Resin recession shall be inspected in accordance with 4.8.5.1.

3.8.11 Lifted lands prior to thermal stress, rework simulation, or bond strength). When types 1, 2, and 3 printed-wiring boards are tested as specified in 4.8.5.11, there shall be no lifted lands on the (as-received) microsection specimens. As-received meaning after fusing but prior to thermal stress, rework simulation, or bond strength testing (see 3.9).

4.8.5.11 Lifted lands (see 3.8.11). Lifted lands on the as-received microsection specimen shall be inspected in accordance with 4.8.5.1.

3.9 Plated-through holes after stress (see 4.8.6) (see figure 8). The three plated-through holes shall be inspected in the vertical cross-section in accordance with 4.8.6. Figure 8 shows the plated-through hole structure evaluation zones. Following stress (3.9.1 through 3.9.3), there shall be no cracks in the internal conductive foils, platings, or coatings. Cracks are permissible in the outer copper foil provided they do not extend into the plated copper. Laminate voids are not evaluated in zone A. Laminate voids greater than 0.003 inch that extend into zone B are a reject. Measling shall not exceed the requirements of IPC-A-600 Class 3.

4.8.6 Plated-through holes (see 3.9). IPC-A-600 states that for class 3, measling shall result in a maximum of 25% reduction between non-common conductors and have a total area equal to or less than 1% of the surface area (each side considered separately).

3.9.1 Thermal stress (types 2 and 3). When a type 2 or 3 specimen is visually inspected in accordance with 4.8.1 and 4.8.1.2 [visual examination and microsectioning], the specimen shall exhibit no cracking of plating, separation of plating and conductors, blistering or delamination in excess of that allowed in 3.5.3 [subsurface imperfections, not cited], and shall be inspected in accordance with 4.8.6.1. Laminate voids in zone B (see figure 8) with the longest dimension of 0.003 inch (0.08mm) shall be permitted provided the conductor spacing is not reduced below the minimum dielectric spacing, laterally or vertically, as shown on the master drawing. Resin recession at the outer surface of the plated-through hole barrel shall be permitted and is not cause for rejection.

4.8.6.1 Thermal stress types 2 and 3 (solder float) (see 3.9.1). The specimens shall be conditioned at 250 F to 300F (121 C to 149 C) for a minimum of 6 hours to remove moisture. (Note: More complex specimens may require longer conditioning time.) After conditioning, place specimens in a dessicator on a ceramic plate to cool to room temperature. The specimens shall then be fluxed (type RMA per MIL-F-14256) and floated in a solder bath of composition Sn60, Sn62, or Sn63 maintained at 550 F ± 10 F (287 C ± 6 C) for a period of 10 +1 –0 seconds. Solder temperature will be measured at a probe depth not to exceed 1.00 inch (25.4mm) from the molten surface of the solder. After thermal stressing, place specimens on a piece of insulator to cool to room temperature. Specimens shall be inspected in accordance with 4.8.1.2.1 and meet the requirements of 3.9.1.

3.9.2 Rework simulation, plated-through holes. Types 2 and 3 printed-wiring boards shall be inspected in accordance with 4.8.6.2. After the fifth cycle of soldering and unsoldering of the test wire, the plated-through hole shall exhibit no plating cracks, blistering, or delamination in excess of that allowed in 3.5.3. Laminate voids in zone B (see figure 8) with the longest dimension of 0.003 inch (0.08mm) or less shall be permitted provided all minimum dielectric requirements are met. Resin recession at the outer surface of the plated-through hole barrel shall be permitted and is not cause for rejection.

4.8.6.2 Rework simulation, plated-through hole (see 3.9.2). Rework simulation of plated-through holes shall be in accordance with IPC-TM-650, method 2.4.36. Following the fifth cycle of soldering and unsoldering of the test wire, the plated-through holes shall be microsectioned and inspected in accordance with 4.8.1.2 [p. A-2] and meet the requirements of 3.9.2. The rework simulation shall be performed after stabilizing of the coupons at temperatures of 59 F to 95 F (15 C to 35 C) and relative humidity of 40 to 85 percent for a period of 24 hours.

3.9.4 Lifted lands (after thermal stress, rework simulation, or bond strength). When types 1, 2, and 3 printed-wiring specimens (which have been subjected to thermal stress, rework simulation, or bond strength) are inspected as specified in 4.8.6.4, the maximum allowance of lifted land from the base material to the outer lower edge of the land shall be 0.003 inch (0.08 mm) on both sides of the hole. There shall be a minimum of 50% of the land bonded on each side of the hole (see figure 9).

4.8.6.4 Lifted lands (see 3.9.4). Specimens, which have been subjected to tests specified in 4.8.6.1, 4.8.6.2, 4.8.6.3, or 4.8.4.4 [thermal stress (types 2 and 3) rework simulation, thermal shock, or bond strength (unsupported hole)], shall be inspected for lifted lands in accordance with 4.8.5.1 for type 2 and 3 and in accordance with 4.8.1.2.1 for type 1.

TABLE I. PLATING AND COATING THICKNESS[1]

Plating material	Surface and through-hole thickness
Gold	0.000050 inch minimum
Nickel	0.0002 inch minimum
Tin-lead	0.0003 inch minimum at the surface as plated
Solder coating	0.0003 inch minimum at crest on the surface as coated

[1] A coupon prior to reflow may be required (see 4.6 and table VII).

TABLE III. PLATING OR COATING THICKNESS[1]

Plating material	Surface and through-hole plating thickness (inch)
Electroless copper	Sufficient for subsequent electrodeposition
Electrolytic copper	0.001 minimum (0.03 mm)

[1] Isolated flaws are permitted down to 0.0008 inch (0.0203 mm). Any isolated areas measuring less than 0.0008 inch (0.0203 mm) shall be treated as a void.

TABLE VII. GROUP A INSPECTION

Inspection	Requirement paragraph	Method paragraph	Production board	Test coupon by board type[1]			AQL (percent defective)	
				1	2	3	Major	Minor
Material	3.4, 3.4.1 thru 3.4.7	—	—	Manufacturer certification			—	—
Visual:	3.5	4.8.2	[2]					
Edges of printed wiring board	3.5.1	4.8.2.1	X	—	—	—	1.0	4.0
Surface imperfections	3.5.2	4.8.2.2	X	—	—	—	1.0	4.0
Subsurface imperf'ns	3.5.3	4.8.2.3	X	—	—	—	1.0	4.0
Marking	3.5.4	4.8.2.4	X	—	—	—	1.0	4.0
Traceability	3.5.4.1	4.8.2.4	X	—	—	—	1.0	4.0
Workmanship	3.5.5	4.8.2.5	X	—	—	—	1.0	4.0
Solderability	3.5.6	4.8.2.6	—	—	—	—	—	—
Surface	3.5.6.1	4.8.2.6.1	[3]	C	—	—	1.0	4.0
Hole	3.5.6.2	4.8.2.6.2	—	—	A	A	1.0	4.0
Thermal stress	3.5.7	4.8.2.7	—	B	—	—	1.0[6]	4.0
Dimensional:	3.6 and 3.6.1	4.8.3	—	—	—	—	1.0	4.0
Hole pattern	3.6.2	4.8.3.1	X	—	—	—	1.0	4.0
Bow and twist	3.6.3	4.8.3.2	X	—	—	—	1.0	4.0
Conductor spacing	3.6.4	4.8.3.3	X	—	—	—	1.0	4.0
Conductor pattern	3.6.5	4.8.3.4	X[7]	—	—	—	1.0	4.0
Layer-to-layer registration	*3.6.6	*4.8.3.5	—	—	[8]	F	1.0	4.0
Annular ring (external):	3.6.7	4.8.3.6	X	—	—	—	1.0	4.0
Unsupported hole	3.6.7.1	4.8.3.6	X	—	—	—	1.0	4.0
Plated-through hole	3.6.7.2	4.8.3.6	X	—	—	—	1.0	4.0
Solder mask thickness	3.6.8	4.8.3.7	X[3]	E[3]	E[3]	E[3]	1.0	4.0
Plating and coating thickness	3.6.9	4.8.3.8	X[3]	C[3]	C[3]	C[3]	1.0	4.0
Physical requirements:	3.7	4.8.4	—	—	—	—	—	—
Solder mask cure and adhesion	3.7.1	4.8.4.1	X[3]	J[3]	J[3]	J[3]	1.0	4.0
Plating adhesion	3.7.2	4.8.4.2	X[3]	C[3]	C[3]	C[3]	1.0	4.0
Conductor edge outgrowth[9]	3.7.3	4.8.4.3	X	—	—	—	1.0	4.0
Construction integrity (microsection)[4]	3.8	4.8.5	—	—	—	—	—	—
Plated-through hole	*3.8.1	*4.8.5.1	—	—	B	B	[4]	[4]
Plated copper thickness	*3.8.2	*4.8.5.2	—	B	B	B	[4]	[4]
Plating voids	*3.8.3	*4.8.5.3	—	B	B	B	[4]	[4]
Conductor thickness	*3.8.4	*4.8.5.4	—	B	B	B	[4]	[4]
Resin smear and etchback	*3.8.5	*4.8.5.5	—	—	—	—	—	—
Hole cleaning (smear removal)	*3.8.5.1	*4.8.5.5	—	—	—	B	[4]	[4]

See footnotes at end of table.

TABLE VII. GROUP A INSPECTION (CONTINUED)

Inspection	Requirement paragraph	Method paragraph	Production board	Test coupon by board type[1]			AQL (percent defective)	
				1	2	3	Major	Minor
Negative etchback	*3.8.5.2	*4.8.5.5	—	—	—	B	4	4
Etchback	*3.8.5.3	*4.8.5.5	—	—	—	B	4	4
Undercutting	*3.8.6	*4.8.5.6	—	B	B	B	4	4
Annular ring (internal)	*3.8.7	*4.8.5.7	—	—	——	B	4	4
Dielectric layer thickness	*3.8.8	*4.8.5.8	—	—	B	B	4	4
Laminate voids	*3.8.9	*4.8.5.9	—	—	B	B	4	4
Resin recession	*3.8.10	*4.8.5.10	—	—	B	B	4	4
Lifted lands	*3.8.11	*4.8.5.11	—	B	B	B	4	4
Plated-through holes	3.9	4.8.6	—	—	—	—	5	—
Thermal stress	*3.9.1	*4.8.6.1 and 4.8.1	—	—	B[4]	B[4]	—	5
Electrical and environmental requirements	3.10	4.8.7	—	—	—	—	—	—
Circuitry	3.10.3	4.8.7.3	—	—	—	—	—	—
Circuitry continuity	3.10.3.2	4.8.7.3.1	X	—	—	—	100% inspection[10]	
Circuit shorts	3.10.3.3	4.8.7.3.2	X	—	—	—	100% inspection[10]	
Repair	3.10.5	4.8.7.5	—	All	All	All	100% inspection	

[1] See MIL-STD-275, and paragraph 1.2.
[2] Visual examination (4.8.1) of production board surface for all three board types (1, 2, and 3).
[3] Test coupon or production board, manufacturer's option coupon shall be processed with production board.
[4] One coupon per panel shall be microsectioned for type 3 boards; the number of coupons to be microsectioned for types 1 and 2 boards shall be based on a statistical sample in accordance with MIL-STD-105 General Inspection level II of the number of panels produced and shall meet an AQL of 2.5 percent defective.
[5] For type 3 boards, microsection 1 coupon per panel 100 percent of the time in any one direction, and microsection perpendicular to that direction on a sampling of the microsectioned coupons based on MIL-STD-105 General Inspection level II with an AQL of 2.5 percent defective. Type 2 boards shall be microsectioned in only one direction.
[6] See 4.7.1.2 of MIL-P-55110.
[7] Inspected prior to lamination.
[8] Production board shall be used for type 2.
[9] May be inspected by examination of microsectioned coupon associated with production board.
[10] If the printed-wiring assembly drawing required the circuitry test to be run with 100 percent inspection on the printed-wiring assembly, a sampling plan (4.7.1.2.1) based on an AQL of 2.5 percent defective shall be used on the bare unassembled printed-wiring board.

TABLE IX. GROUP B INSPECTION

Inspection	Requirement paragraph	Method paragraph	Test coupon by type[1]		
			1	2	3
Bond strength	3.7.4	4.8.4.4	B	—	—
Rework simulation	3.9.2	4.8.6.2	—	B	B
Moisture and insulation resistance	3.10.1	4.8.7.1	E	E	E
Dielectric withstanding voltage	3.10.2	4.8.7.2	E	E	E

[1] See MIL—STD-275 and 1.2 herein.

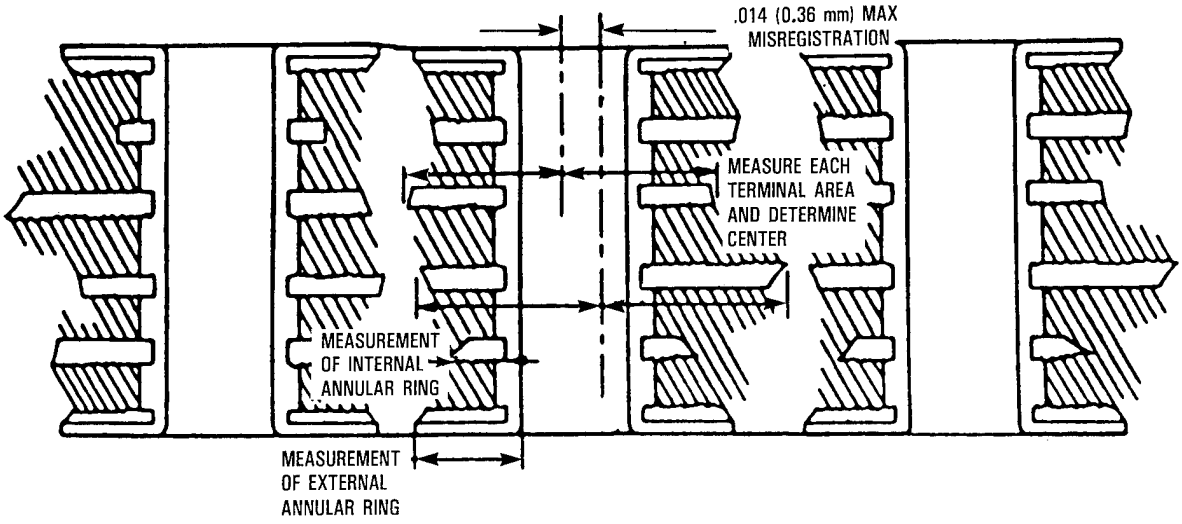


Figure A-1. Layer-to-layer registration and annular ring measurement.

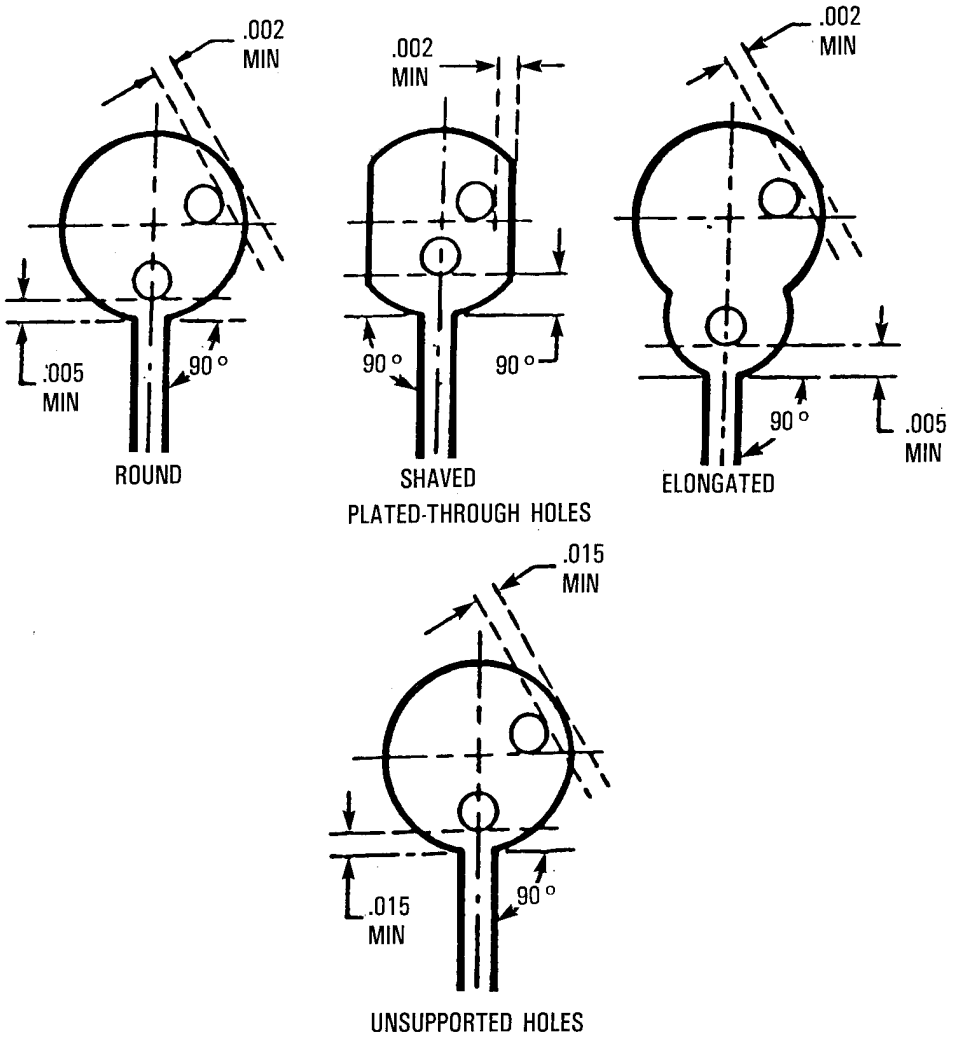
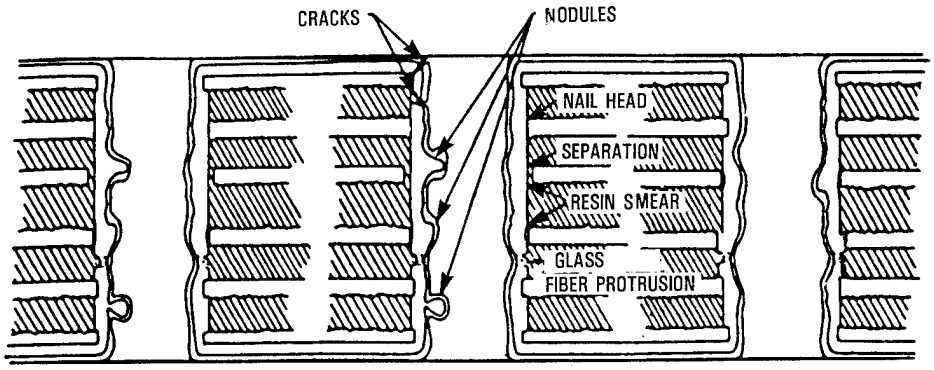


Figure A-2 Land areas (minimum annular ring, external).



TYPE OF DEFICIENCY	TYPE(S) OF BOARD TO WHICH DEFICIENCY APPLIES
CRACKS	2, 3
NODULES	2, 3
NAIL HEAD	3
SEPARATION	3
RESIN SMEAR	3
GLASS FIBER PROTRUSION	2, 3

Figure A-3. Plated-through hole workmanship (deficiencies).

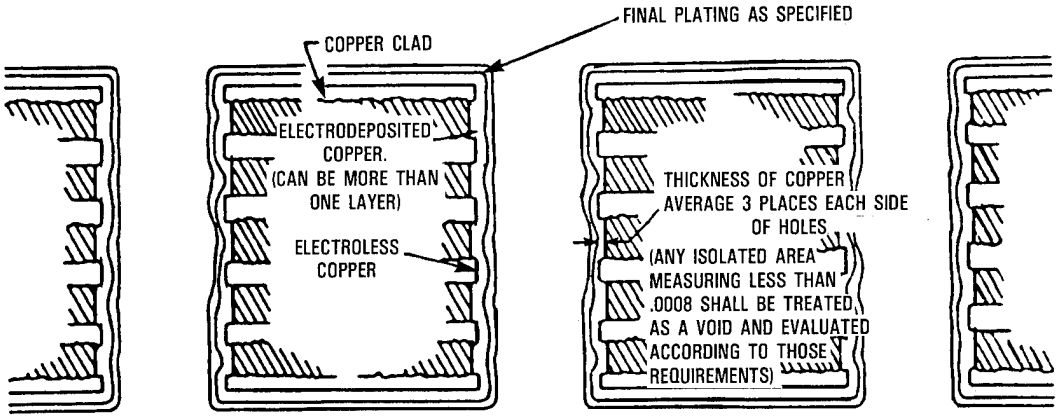


Figure A-4. Plating thickness.

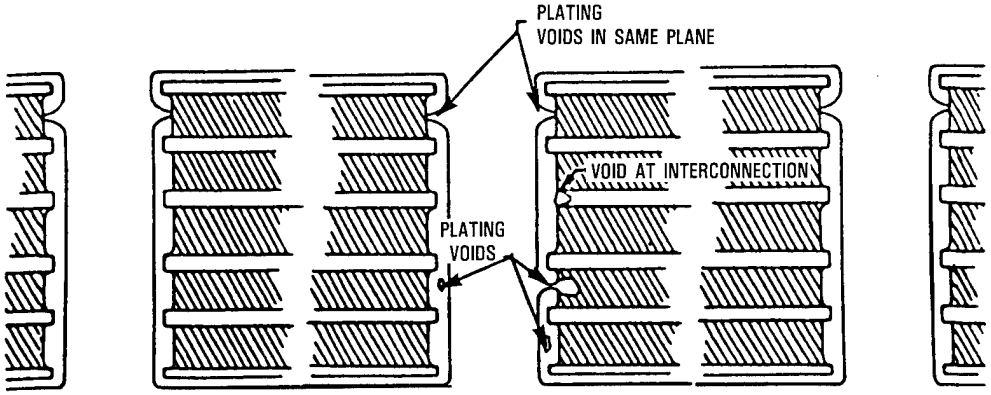
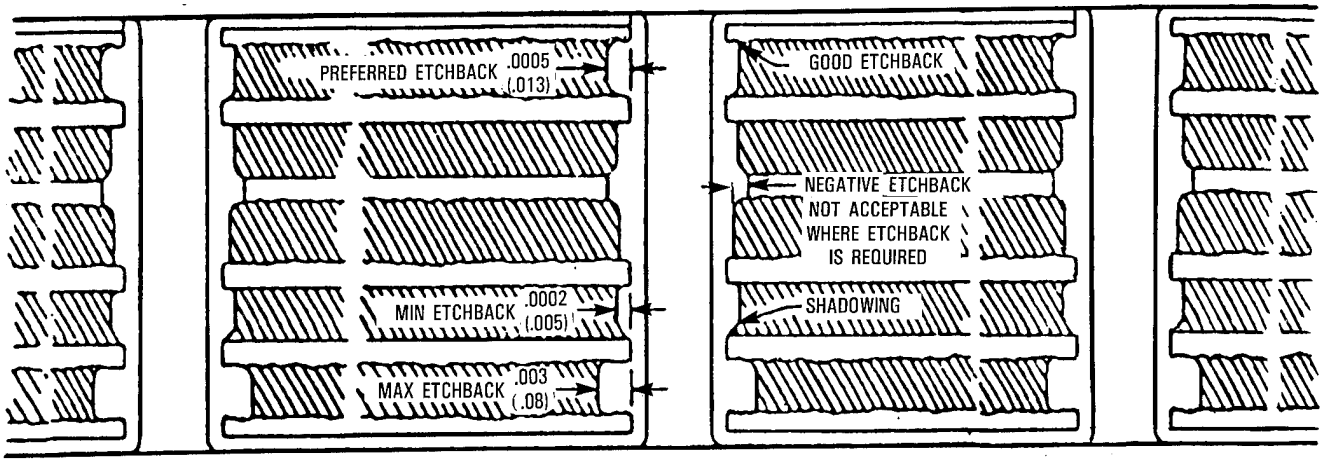


Figure A-5 Typical plating voids.



NOTES:
1. DIMENSIONS ARE IN INCHES.
2. METRIC EQUIVALENTS ARE GIVEN FOR GENERAL INFORMATION ONLY.
3. METRIC EQUIVALENTS ARE IN PARENTHESES.

Figure A-6. Forms of etchback.

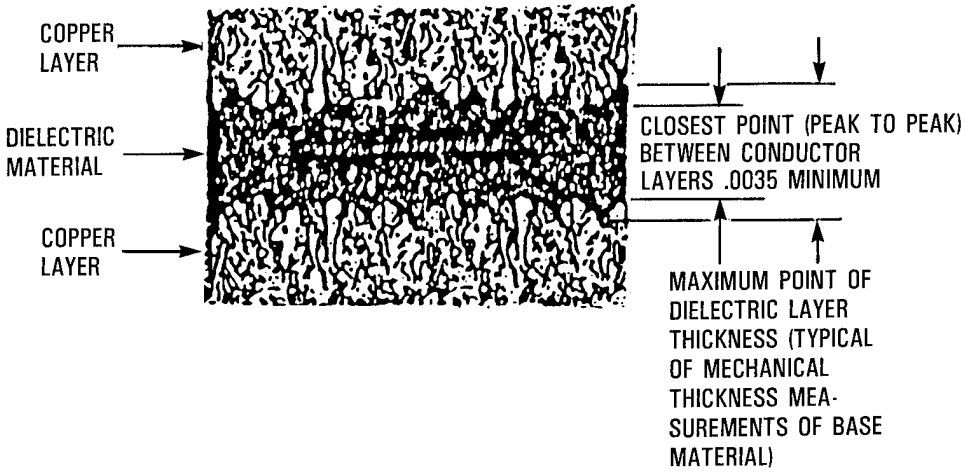
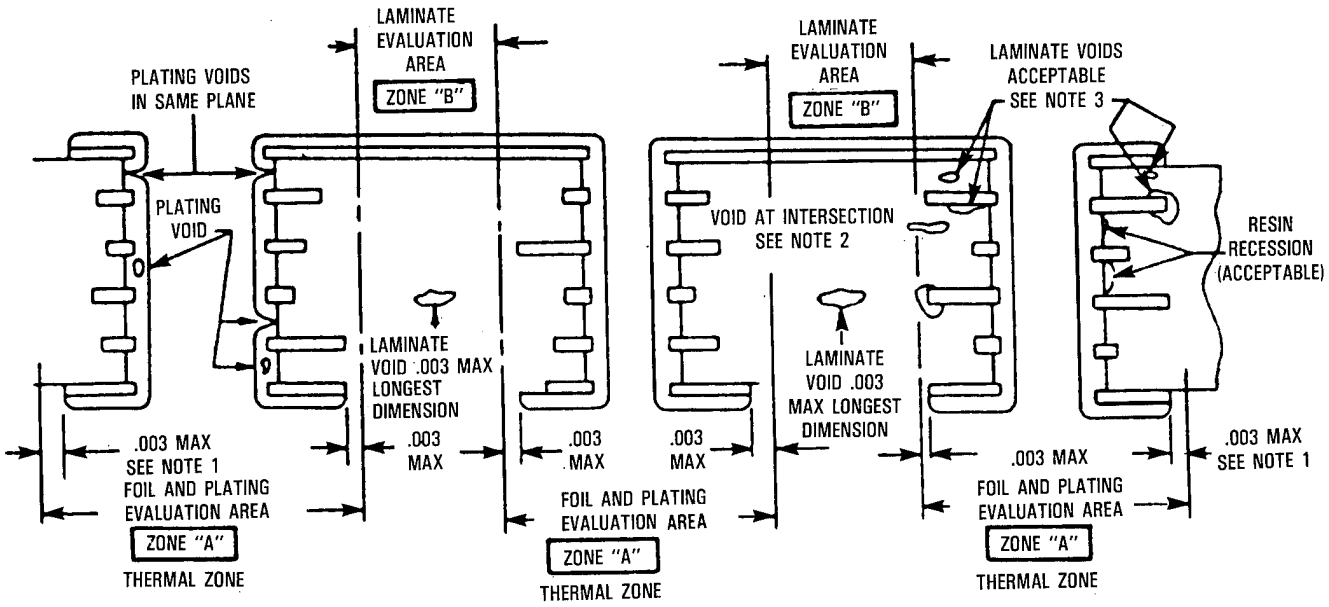


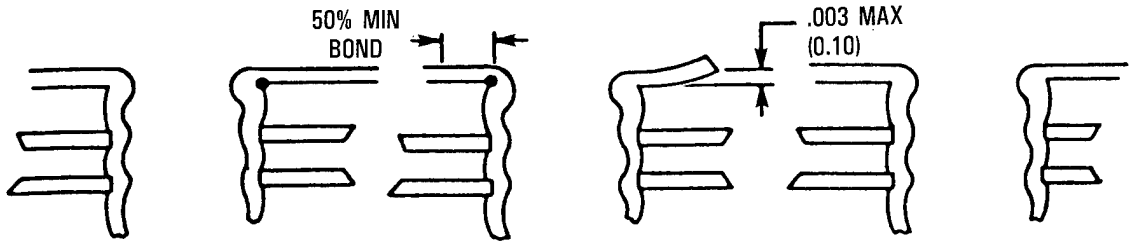
Figure A-7. Dielectric layer thickness measurement.



NOTES:

1. TYPICALLY BEYOND LAND EDGE MOST RADIALLY EXTENDED.
2. VOID AT INTERSECTION OF ZONE A AND ZONE B. LAMINATE VOIDS GREATER THAN .003 (0.08 mm) IN LENGTH WHICH EXTEND INTO THE LAMINATE EVALUATION AREA ARE REJECTABLE.
3. LAMINATE VOIDS ARE NOT EVALUATED IN ZONE A. LAMINATE VOIDS GREATER THAN .003 (0.08 mm) THAT EXTEND INTO ZONE B ARE REJECTABLE.
4. DIMENSIONS ARE IN INCHES.
5. METRIC EQUIVALENTS ARE GIVEN FOR GENERAL INFORMATION ONLY.

Figure A-8. Typical plated-through hole cross section (3 hole sample) (after thermal stress and rework simulation.



NOTES:

1. DIMENSIONS ARE IN INCHES.
2. METRIC EQUIVALENTS ARE GIVEN FOR GENERAL INFORMATION ONLY.
3. METRIC EQUIVALENTS ARE IN PARENTHESES.

Figure A-9. Lifted lands.

APPENDIX B

A PROCEDURE FOR METALLOGAPHIC PREPARATION AND EXAMINATION OF MULTILAYER PRINTED WIRING BOARD COUPONS

Note 1: The accuracy and reliability of this method are highly dependent on individual technique and skill. Experienced personnel and a microscope of good quality are prerequisites to accurate evaluation. This suggested method assumes a general knowledge of metallographic techniques but no prior experience with printed-wiring boards. There are, of course, numerous variations of method which produce acceptable results, and these may be employed according to the level of experience of the metallographer concerning specimens of this nature.

Note 2: In addition to the specific procedure listed herein, reference is also made to ASTM Method E2 "Preparation of Micrographs of Metals and Alloys," ASTM Method E3 "Preparation of Metallographic Specimens," ASTM Method B-487 "Measurement of Metal and Oxide Thicknesses by Microscopical Examination of a Cross Section, and IPC-TM-650, Method 2.1.1, "Microsectioning,"

Description of Specimen: Cut specimens from test coupon so that they contain at least three holes of the smallest size used for component leads. Holes should have pads at each layer. For additional evaluation specimens may be cut parallel to the surface. For examination after thermal stress, test coupons must have been subjected to all normal manufacturing steps, including solder reflow when specified, and to the thermal stress (solder float) test according to MIL-P-55110D, Paragraph 4.8.6. For layer-to-layer registration evaluation, cut one hole parallel to the board length and one hole perpendicular to it. A low-speed ($<$ = 300 rpm) cut-off wheel with a diamond blade, using suitable cutting fluid, is preferred to minimize damage to the coupon. A jeweler's hacksaw may also be used, taking care not to overheat the board. Regular shop-sized hacksaws are not to be employed. The cut should be made adjacent to the conductor pads, not through the hole itself.

Test Equipment/Apparatus:

1. For Solder Float Testing:
   - Solder pot capable of maintaining 550 F ± 10 F (287 ± 6 C)
   - Oven capable of maintaining 275 F ± 25 F (135 ± 14 C)
   - Dessicator
   - Insulating plate (such as a firebrick or slab of ceramic)
   - Solder, Sn60, Sn62, or Sn63
   - Flux, type RMA of MIL-F-14256
   - Tongs for handling hot specimens, or wire small enough to fit through the holes on the coupon
2. For sectioning and Encapsulation:
   - Glass plate 5 in. x 7 in. or aluminum weighing dishes 2½ in. dia. approx.
   - Aluminum or Bakelite rings 1 in. or 1¼ in.
   - Silicone release agent
   - Silicone vacuum grease
   - Room-temperature curing potting material (for example, Dow Corning Epon 828 with TETA catalyst, mix ratio 10:1)
   - Wooden spatulas
   - Plastic cups

   Low-speed cut-off wheel, or jeweler's hacksaw
   - Engraver
   - 240 grit abrasive
   - Double coated tape, stainless steel or plastic spring clips
3. For Grinding, Polishing and Examination:
   - Metallographic polishing table–3 wheels preferred for manual polishing or automatic setup
   - 240, 320, 400, and 600 grit abrasive papers, for use with water or other coolant
   - 1.0, 0.3, and 0.05 micron alumina slurries, or 6 and 1 micron diamond pastes
   - Polishing cloths (low napped and napped)
   - Chemical etchants (for example, 3% hydrogen peroxide and concentrated ammonium hydroxide)
   - Metallurgical microscope with camera accessories capable of 50 - 400X magnification
   - Filar eyepiece or graduated reticle
   - Low-power binocular microscope (7 - 25X)

Procedure for Solder Float Testing:

Do no: wet cutting or grinding between conditioning and solder floating. If solder floating does not immediately follow conditioning, store conditioned coupons in a dessicator. Hot specimens may be handled with tongs, or a short length of tinned copper wire of a suitable size may be inserted into a hole which is not to be evaluated and formed into a handle at 90 degrees to the plane of the coupon. If the handle is about three inches long, it will remain cool enough during the solder float to be picked up bare-handed. Proceed with conditioning and solder floating as detailed in 4.8.6 of MIL-P-55110 (p. A-5 this document).

Procedure for Encapsulation:

NOTE: SPECIMEN ENCAPSULATION PROCEDURES INVOLVING TEMPERATURES IN EXCESS OF 100 C OR PRESSURE MOLDING APPARATUS ARE PROHIBITED. (The laminate will soften and flow under these conditions, changing the original condition of the coupon, and rendering the examination and evaluation procedure invalid.)

1. Clean glass plate and rings and dry thoroughly. If using aluminum weighing dishes, no cleaning is necessary. Use one dish for each ring.
2. Apply strip of double-coated tape to plate or dish to support specimen if spring clips are not used. Apply thin film of release agent to glass plate (and ring if desired). No release agent is necessary on the aluminum dishes. Smooth one edge of ring on 400 grit abrasive paper, lightly grease this edge with a silicone vacuum grease to prevent leakage of the mounting material, and press this edge of the ring onto the glass plate or dish.
3. Grind the long edge of the perpendicular specimen until the edges of the conductor pads appear and the specimen will stand on edge on a flat surface. Use 240 grit abrasive with ample coolant. This step may not be necessary for specimens cut with a diamond blade on low-speed wheel. Alternatively, this step may be performed after encapsulation, and continued until a plane just short of the center of the holes is reached (to allow room for subsequent fine grinding steps), checking progress frequently with a low-power microscope so as not to grind beyond the center of the holes.
4. Stand specimen on edge on double-coated tape or insert into spring clip with the plated-through hole edge down. Avoid covering holes with clip. For parallel specimens omit the tape or clip and lay specimen flat on the glass plate inside the ring. One or more specimens may be placed in the same mount, making sure that those in one mount have been pre-cut or preground so that the centerline of all holes is in the same plane. As-received and solder float tested coupons may be mounted together if desired. Multiple specimens should be spaced apart or offset to facilitate flow of the mounting material into the holes. Coupon identification may be maintained by means of adhesive labels on the sides of the rings, on the glass plate next to them, or by engraving (with a ball point pen) on the bottom of the aluminum dish outside of the ring.
5. Mix potting material and pour to one side of the specimen until it flows through the holes. Support the specimen in vertical position if necessary. Continue pouring until ring is full. Avoid entrapment of air. If using a viscous epoxy, it is helpful to outgas the mixture for a few minutes in a low-vacuum apparatus prior to pouring, or to pour a small amount into the mold and then outgas until bubbling slackens. Then add additional epoxy mixture to fill the mold. For the Epon 828/TETA mixture, the filled ring mold may be placed in an oven held at 50 C for a period of about 2 hours. The heat thins the mixture so that it flows well into the holes and deaerates itself without vacuum degassing.
6. Allow specimen to cure at room temperature. Accelerated curing at elevated temperature is permissible following manufacturer's instructions, provided the temperature does not exceed 100 C and provided cracking and distortion do not occur. The Epon 828/TETA mixture held at 50 C as described above will be sufficiently cured for grinding and polishing after an additional two hours or so at that temperature or at room temperature.
7. Identify specimen promptly by engraving. For multiply mounted specimens, adequate care should be taken to identify each specimen.

Grinding and polishing:

1. Rough grind face of specimen to the approximate center of the plated-through holes using 240, 230, 400 and 600 grit papers in that order, using adequate lubrication and/or coolant. Silicon carbide papers used with plenty of water work well. Do not omit any steps. When changing grit size, rotate the specimen 90 degrees and grind on the finer grit for at least twice the length of time it takes to remove the scratches caused by the coarser grit. Rinse specimen well in tap water between steps.
2. Flush away all residue using room temperature or comfortably warm tap water. Wash hands to avoid carrying over coarse grit. Ultrasonic cleaning in plain or soapy water may be used.
3. Rough polish using a slurry of 1.0 micron alumina in distilled water on a nylon or other napless cloth until all scratches from the 600 grit are removed. Follow with 0.3 micron alumina slurry on another nylon or softer cloth. Final polish using 0.05 micron alumina slurry on a napped cloth. Rinse specimen (or ultrasonically clean) and wash hands thoroughly between steps. While polishing, rotate specimen 360 degrees about the axis of the wheel and opposite to the direction of rotation of

the wheel, keeping the face of the specimen flat on the wheel. If the specimen has been ground correctly, a few minutes on each wheel should suffice. Verify completeness of each step using microscope at 50 - 100X. Prolonged polishing may result in excessive edge rounding, pitting, or other artifacts. NOTE: 6 micron and 1 micron diamond on nylon may be substituted for the coarser aluminas. Automatic equipment may be used if available.

4. Rinse in warm tap water and/or alcohol and dry in warm forced air.

Examination

1. Examine multilayer board innerplane-to-barrel interfaces at 100X minimum (200X preferred) before any chemical etching. The interface should not be distinguishable in the unetched condition. Any evidence of a demarcation line seen prior to etching indicates a lack of true metallurgical bonding between the barrel plating and the end of the foil layers and should be noted as a defect. It is important to make this examination before etching because the plating layer(s) will be delineated by the etching, and a fine line defect or very narrow separation can easily be masked by this feature. If in doubt whether a feature is real or is a polishing artifact, repeat the two final polishing steps and re-examine.

2. Chemically etch the specimen to reveal plating microstructure. A 1:1 solution by volume of concentrated ammonium hydroxide and 3% hydrogen peroxide will etch copper but not attack tin-lead solder. Solution must be freshly prepared (it will not keep more than a few minutes) and may be applied by swabbing gently for about 5 - 10 seconds. Rinse well with warm water or alcohol and dry with warm forced air. The presence of an orange stain indicates that the chemicals must be replaced.

3. If desired, a thin film (300 - 500 angstroms) of gold or other metal may be applied by vapor deposition or sputtering on the polished and etched specimen to enhance the reflectance of the laminate. This facilitates photomicrography of the specimen and the detection of laminate voids.

4. Proceed with the remainder of the examinations and measurements as detailed in MIL-P-55110D.

5. Maintain a written log containing date, board manufacturer, intended use, part and serial numbers, results of evaluation, evaluator's name, representative photographs of coupons, and other such information as may be appropriate.

APPENDIX C

PRINTED WIRING BOARD TEST REPORT
PLATED-THROUGH HOLE EVALUATION

Report No.: _____ Project: _____ Date _____

PWB Part No./Serial No.: _____ Mfr.: _____

Submitted by: _____ Code _____ Phone _____

Evaluated by: _____

MIL-P-55110D _____ NHB 5300.4 (3I) _____ Result: _____

Approved by: _____ Date: _____

TEST	REQUIREMENT	RESULT As-Received	RESULT Solder Float
A. Dimensional			
1. Plating Thickness	0.001" min	_____	
2. Annular Ring (Ext.)	0.002" min	_____	
3. Annular Ring (Int.)	0.002" min	_____	
4. Nailheading	$< 1.50\ T_{FOIL}$	_____	
5. Registration	0.014" max	_____	
*6. Thermal plane/PTH Space	0.004" min	_____	
7. Dielectric Thickness	0.0035" min	_____	
8. Etchback (if specified)	0.0002" min 0.003" max	_____	
*9. Smear Removal (if no etchback specified)	−0.0005" min 0.001" max	_____	_____
**10. Laminate Voids	0.003" max	_____	_____
**11. Resin Recession	0.003" max < 40% Cum. Diel. Thk.	_____	_____
*12. Lifted Lands	None (AR); 0.003" max Lift, 50% minimum bond (SF)	_____	_____
B. Plating and Foil Quality (Before etching)			
†1. Cracks	None	_____	_____
††2. Voids	3 max. ea.hole; no 2 in same plane	_____	_____
3. Separations	None		
a. Between plating layers		_____	_____
b. At foil/barrel interfaces		_____	_____
4. Resin Smear	None	_____	_____
C. Plating and Foil Quality (after etching)			
†1. Cracks	None	_____	_____

D. Remarks: _____

_____

_____

E. Illustrations. Append on separate sheet photomicrographs at suitable magnifications illustrating A) typical areas of accepted coupons, or B) defects which warranted rejection. For accepted coupons, one photomicrograph at 50X and one at 200X are suggested. Number and magnifications will vary with defect types.

NOTES:

*Requirement of MIL-P-55110D, not addressed in NHB 5300.4(3I)

**Not evaluated in Zone A under MIL-P-55110D after thermal stress; criteria of NHB 5300.4(3I) are the same for both conditions.

†MIL-P-55110D permits cracks in the outer foil layers (but not penetrating the barrel plating) after solder float. NHB 5300.4(3I) does not.

††Criteria of MIL-P-55110D. NHB 5300.4(3I) permits no plating voids.

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15. Supplementary Notes

16. Abstract

This work is an illustrated handbook containing the rationale and procedure for the evaluation of multilayer printed wiring board construction integrity with respect to plated-through holes in accordance with the requirements of MIL-P-55110D, "Printed Wiring Boards." It is intended as a practical aid for those concerned with determining the construction integrity of multilayer boards for high reliability applications. Photomicrographs of cross-sectioned holes illustrate defect types, acceptable and unacceptable conditions, and methods of measurement. A procedure for specimen preparation is given, and appropriate paragraphs of the military specification are included and explained.

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